Display Elektronik GmbH

DATA SHEET

STANDARD OLED/PLED

DEP 160128A1 - RGB

Product Specification ***Version : 12***

06.07.2017

History of Version

Version	Contents	Date	Note
01	NEW VERSION	08.07.2010	SPEC.
02	Modify module lifetime.	23.02.2012	
03	UPDATE Quality Assurance、Reliability ADD Precautions for Handling、Precautions for Electrical、Precautions for Storage	21.08.2012	
04	Modify Cover page	17.10.2012	
05	Modify Quality Assurance、Power Supply For OLED Module And Panel Layout Diagram	04.02.2013	
06	Modify Electrical Characteristics	19.03.2013	
07	Modify Drawing	05.07.2013	
08	Modify Reliability	18.02.2014	
09	Modify FPC layout and release IDD value	11.12.2014	
10	Modify Drawing	16.09.2015	
11	Modify History of Version、Absolute Maximum Ratings、Optical Characteristics、Precautions for Storage	09.05.2017	
12	Modify Electrical Characteristics-VCC=16.0V(Min)	06.07.2017	

C O N T E N T S

1. Numbering System

2. General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	160x128	dots
Module dimension (L*W*H)	42.7*65*2.025	mm
Active area	35.015*28.012	mm
Dot size	0.048(W)x0.199(H)	mm
Dot pitch	0.073(W)x0.219 (H)	mm

(2) Controller IC: SSD1353 Controller

(3) Temperature Range

Operating	-40 ~ +70°C
Storage	-40 ~ +85°C

3. Absolute Maximum Ratings

Item	Symbol	Condition	Min	Typ	Max	Unit
Operating Temperature	TOP		-40	—	+70	°C
Storage Temperature	TST		-40	—	+85	°C
Humidity					85	%
Supply Voltage For Logic	VDD		2.4	—	3.5	V
Supply Voltage For Panel	VCC		10		20	
Operating life time		80cd/m², 50% checkerboard	12000(1)			Hrs
Operating life time		60cd/m², 50% checkerboard	16000(2)			Hrs

Note:

(A) Under Vcc = 17V, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 80 cd/m² :

- Master contrast setting : 0x0f
- Frame rate : 85Hz
- Duty setting : 1/128

(2) Setting of 60 cd/m² :

- Master contrast setting : 0x0b
- Frame rate : 85Hz
- Duty setting : 1/128

(C) Lifetime should be counted once shipping out from our warehouse . But the exact lifetime must depend on customer's operation enviornment and application.

4. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	–	2.4	3.3	3.5	V
Supply Voltage For Panel	Vcc-V_{SS}	–	16.0	17	17.5	V
Input High Vol	V_{IH}	–	0.8V_{DD}	–	V_{DD}	V
Input Low Vol	V_{IL}	–	0	–	0.2V_{DD}	V
Output High Vol	V_{OH}	–	0.9V_{DD}	–	V_{DD}	V
Output Low Vol.	V_{OL}	–	0	–	0.1V_{DD}	V
Supply Current For Logic (with built-in positive voltage)	I_{DD}	–	–	280	–	mA
Operating current for V_{CC} (No panel attached)	I_{CC}	Contrast=FF		8.9	10	mA

5. Optical Characteristics

Item	Min.	Typ.	Max.	Unit
View Angle	160	–	–	deg
Dark Room contrast	2000:1	–	–	–
Response Time	–	10	–	us
Pixel Luminance	60	80	–	cd/m^2
CIEx(White)	0.27	0.31	0.35	CIE1931
CIEy(White)	0.29	0.33	0.37	CIE1931
CIEx(Red)	0.62	0.66	0.70	CIE1931
CIEy(Red)	0.29	0.33	0.37	CIE1931
CIEx(Green)	0.26	0.30	0.34	CIE1931
CIEy(Green)	0.59	0.63	0.67	CIE1931
CIEx(Blue)	0.10	0.14	0.18	CIE1931
CIEy(Blue)	0.14	0.18	0.22	CIE1931

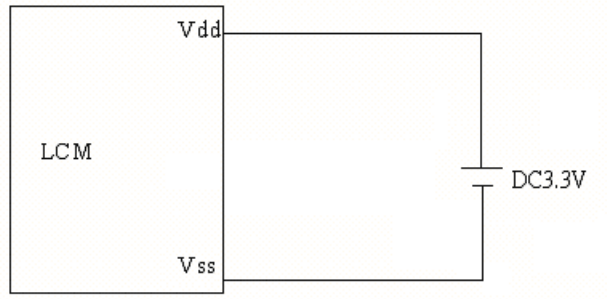
6. Interface Pin Function

Pin No.	Symbol	Level	Description
1	Vss	0V	Ground
2	Vdd	3.3V	Supply voltage for logic
3	CS	H/L	Chip select pin
4	/RES	H/L	Hardware Reset pin
5	D/C	H/L	H: Data; L: Command.
6	RW	H/L	8080: data write enable pin 6800: Read/Write select pin
7	E	H/L	8080: data read enable pin 6800: Read/Write enable pin
8	DB0	H/L	Data bus line
9	DB1	H/L	Data bus line
10	DB2	H/L	Data bus line
11	DB3	H/L	Data bus line
12	DB4	H/L	Data bus line
13	DB5	H/L	Data bus line
14	DB6	H/L	Data bus line
15	DB7	H/L	Data bus line
16	DISF	H/L	DISF: VCC Voltage ON/OFF

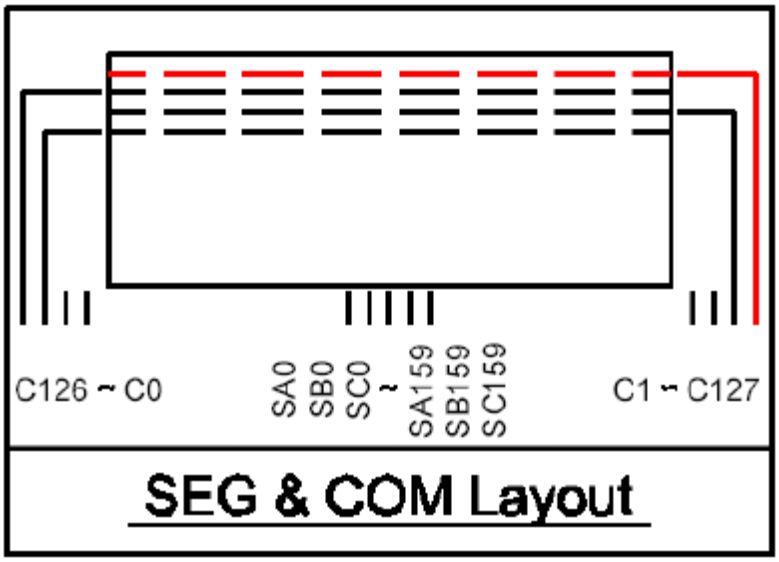
Default:8080 series interface

7. Power Supply For OLED Module And Panel Layout Diagram

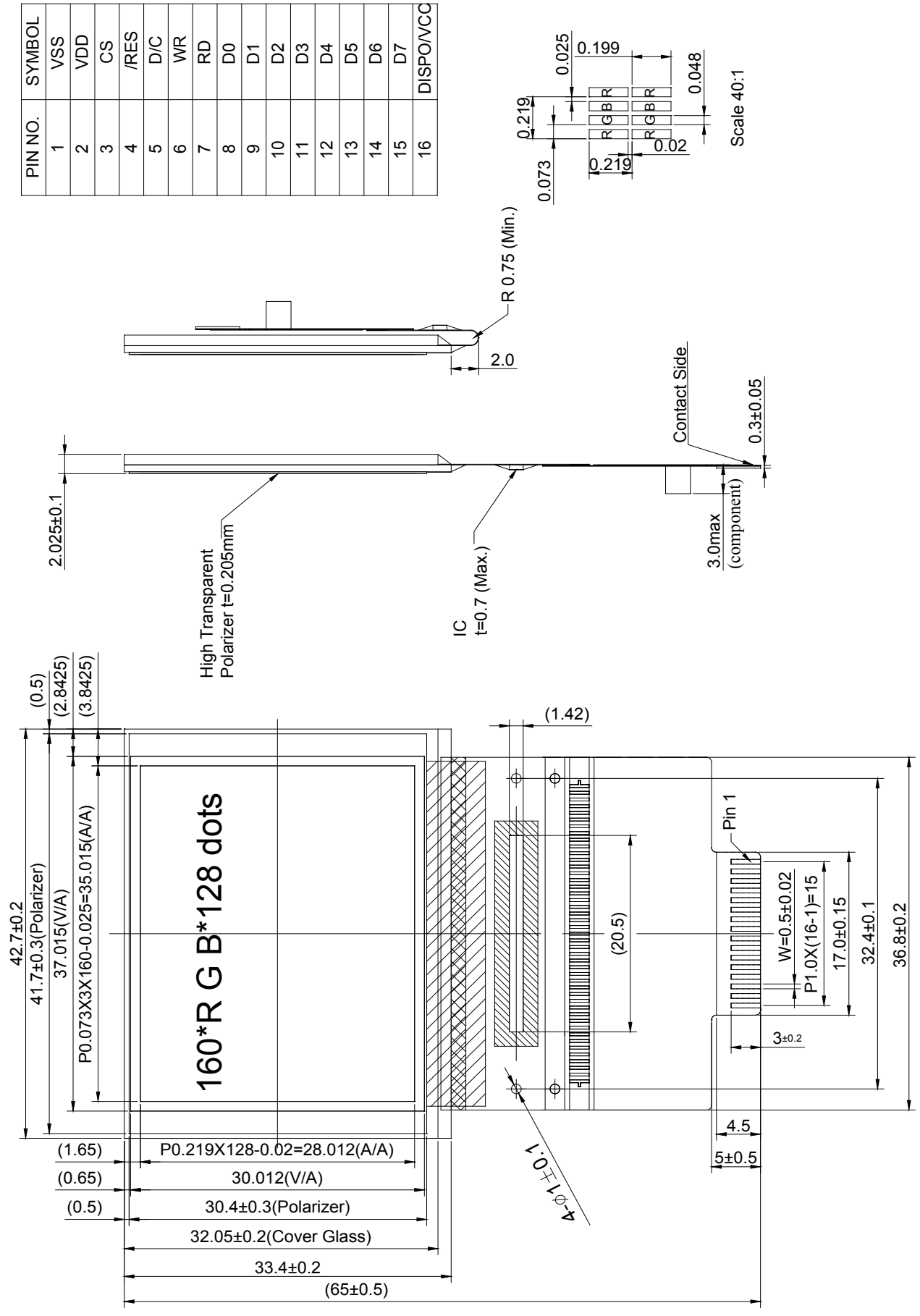
(Optional) LCM operating on " DC 3.3V " input with external positive voltage.



Panel Layout Diagram



8. Drawing

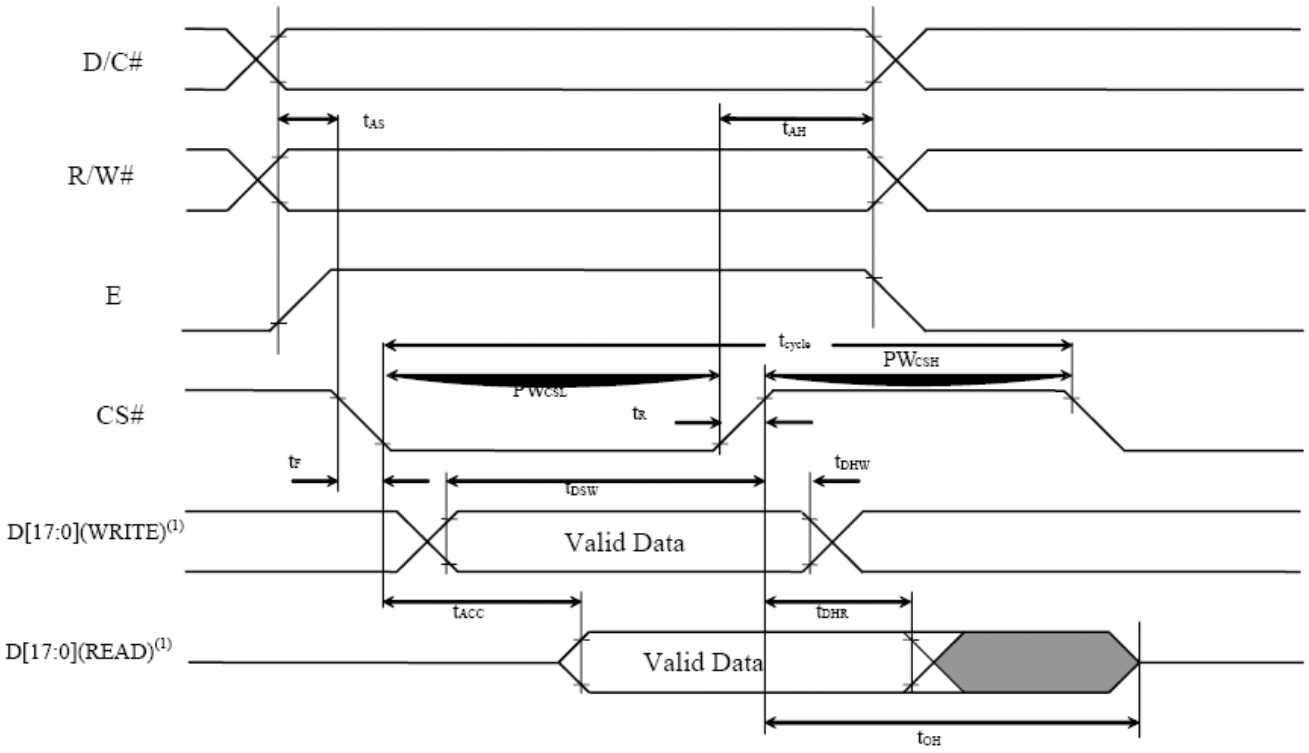

PIN NO. SYMBOL
1 VSS
2 VDD
3 CS
4 /RES
5 D/C
6 WR
7 RD
8 D0
9 D1
10 D2
11 D3
12 D4
13 D5
14 D6
15 D7
16 DISPO/VCC
0.025
0.199
0.048
0.219
0.02
0.073
Scale 40:1
R 0.75 (Min.)
2.0
Contact Side
0.3±0.05
2.025±0.1
High Transparent
Polarizer t=0.205mm
IC
t=0.7 (Max.)
3.0max
(component)
(0.5)
(2.8425)
(3.8425)
(1.42)
Pin 1
42.7±0.2
41.7±0.3(Polarizer)
37.015(V/A)
P0.073X3X160-0.025=35.015(A/A)
160*R G B*128 dots
(20.5)
W=0.5±0.02
P1.0X(16-1)=15
17.0±0.15
32.4±0.1
36.8±0.2
3±0.2
4.5
5±0.5
4-φ1.1±0.1
(1.65)
P0.219X128-0.02=28.012(A/A)
(0.65)
30.012(V/A)
(0.5)
30.4±0.3(Polarizer)
32.05±0.2(Cover Glass)
33.4±0.2
(65±0.5)

9. SSD1353 controller data

9.1 Timing Characteristics

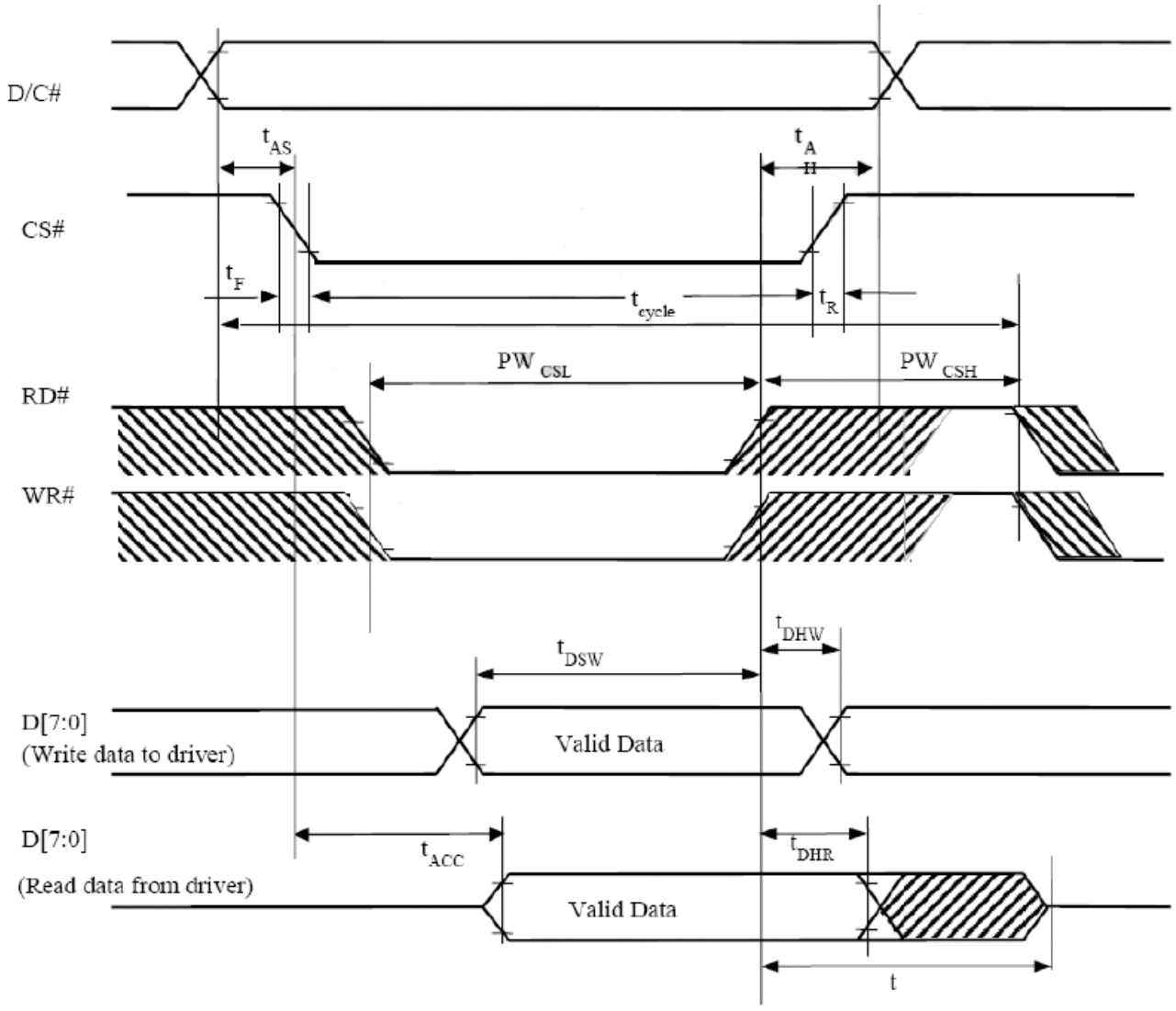
6800 MPU Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



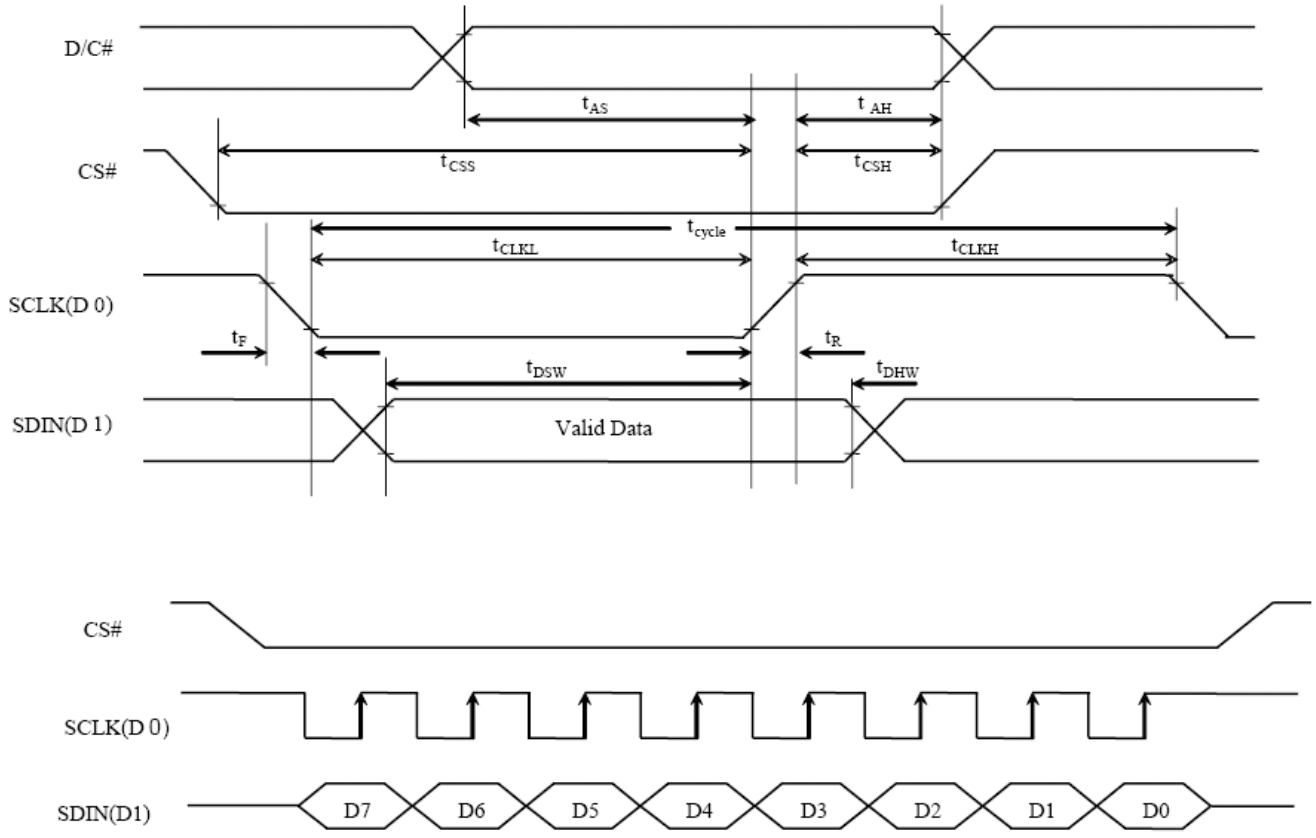
8080 MPU Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns



Serial Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



9.2 Display Control Instruction

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1 1	15 A[7:0] B[7:0]	0 A_7 B_7	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Set Column start and end address A[7:0]: Set start column address from 00d-159d [reset= 0d (00h)] B[7:0]: Set end column address from 00d-159d [reset= 159d (9Fh)]
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1 1	75 A[7:0] B[7:0]	0 A_7 B_7	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	Set Row start and end address A[7:0]: Set start row address from 00d-131d [reset= 0d (00h)] B[7:0]: Set end row address from 00d-131d [reset= 131d (83h)]
0 1	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast for Color "A"	Set contrast for all color "A" segment (Pins :SA0 – SA159) A[7:0] valid range: 00d to 255d [reset=128d (80h)]
0 1	82 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Contrast for Color "B"	Set contrast for all color "B" segment (Pins :SB0 – SB159) A[7:0] valid range: 00d to 255d [reset=128d (80h)]
0 1	83 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Contrast for Color "C"	Set contrast for all color "C" segment (Pins :SC0 – SC159) A[7:0] valid range: 00d to 255d [reset=128d (80h)]
0 1	87 A[3:0]	1 *	0 *	0 *	0 *	0 A_3	1 A_2	1 A_1	1 A_0	Master Current Control	Set master current attenuation factor A[3:0] can be set from 00d to 15d corresponding to 1/16, 2/16… to 16/16 attenuation. [reset= 15d (0Fh)]

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1	8A A[1:0]	1 0	0 0	0 0	0 0	1 0	0 0	1 A_1	0 A_0	Set Second Pre-charge speed	Set Second Pre-charge speed A[1:0]= 00b, Second Pre-charge speed =slowest A[1:0]= 01b, Second Pre-charge speed =slow A[1:0]= 10b, Second Pre-charge speed =normal [reset] A[1:0]= 11b, Second Pre-charge speed =Fast
0 1	A0 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Remap & Color Depth setting	Set driver remap and color depth A[0]=0, Horizontal address increment [reset] A[0]=1, Vertical address increment A[1]=0, RAM Column 0 to 159 maps to Pin SEG (SA,SB,SC) 0 to 159 [reset] A[1]=1, RAM Column 0 to 159 maps to Pin SEG (SA,SB,SC) 159 to 0 A[2]=0, normal order SA,SB,SC (e.g. RGB) [reset] A[2]=1, reverse order SC,SB,SA (e.g. BGR) A[3]=0, Disable left-right swapping on COM [reset] A[3]=1, Set left-right swapping on COM A[4]=0, Scan from COM0 to COM[N –1] [reset] A[4]=1, Scan from COM[N-1] to COM0. Where N is the multiplex ratio. A[5]=0, Disable COM Split Odd Even [reset] A[5]=1, Enable COM Split Odd Even Refer to Figure 10-5 for details. A[7:6] = 00; 256 color format A[7:6] = 01; 65k color format [RESET] A[7:6] = 10; 256k color format A[7:6] = 11; 256k color 16-bit format 2 If 9-/18-bit mode is selected, color depth will be fixed to 256k regardless of the setting. Refer to Table 8-7 for details.
0 1	A1 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set display start line register by Row A[7:0]: from 00d to 131d [reset = 0d (00h)] **Note** (1) A[7:0] must be set to 0 when using A3h command.
0 1	A2 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical offset by COM A[7:0]: from 00d to 131d [reset = 0d (00h)]
0 0 0 0	A4 A5 A6 A7	1 1 1 1	0 0 0 0	1 1 1 1	0 0 0 0	0 0 0 0	1 1 1 1	0 0 1 1	0 1 0 1	Set Display Mode	A4h=Normal Display [reset] A5h=Entire Display ON, all pixels turn ON at GS63 A6h=Entire Display OFF, all pixels turn OFF A7h=Inverse Display

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1	A8 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 Mux N = A[7:0] from 15d to 131d (i.e.16MUX -132 MUX) A[7:0] from 00d to 14d are invalid entry [reset= 131d (83h)]
0 1 1 1 1 1	AB A[7:0] B[7:0] C[7:0] D[7:0] E[4:0]	1 A_7 B_7 C_7 D_7 *	0 A_6 B_6 C_6 D_6 *	1 A_5 B_5 C_5 D_5 *	0 A_4 B_4 C_4 D_4 E_4	1 A_3 B_3 C_3 D_3 E_3	0 A_2 B_2 C_2 D_2 E_2	1 A_1 B_1 C_1 D_1 E_1	1 A_0 B_0 C_0 D_0 E_0	Dim Mode setting	Configure dim mode setting A[7:0] = Reserved. (Set as 00h) B[7:0] = Contrast setting for Color A, valid range 0 to 255d. C[7:0] = Contrast setting for Color B, valid range 0 to 255d. D[7:0] = Contrast setting for Color C, valid range 0 to 255d. E[4:0] = Pre-charge voltage setting, valid range 0 to 31d.
0 0 0	AC AE AF	1 1 1	0 0 0	1 1 1	0 0 0	1 1 1	1 1 1	0 1 1	0 0 1	Set Display ON/OFF	ACh = Display ON in dim mode AEh = Display OFF (sleep mode) [reset] AFh = Display ON in normal mode Refer to Figure 10-12 for transitions between different modes
0 1	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Phase 1 and 2 period adjustment	A[3:0] : Phase 1 period in N DCLKs. 3~31 DCLKs allowed as follow: A[3:0] Phase 1 period 0000 invalid 0001 3 DCLKs 0010 5 DCLKs 0011 7 DCLKs 0100 9 DCLKs [reset] : : 1111 31 DCLKs A[7:4] : Phase 2 period in N DCLKs. 2~15 DCLKs allowed. A[7:4] Phase 2 period 0000 invalid 0001 invalid 0010 2 DCLKs 0011 3 DCLKs : : 0111 7 DCLKs[reset] : : 1111 15 DCLKs

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1	B3 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Display Clock Divider / Oscillator Frequency	A[3:0] Divider DCLK is generated from CLK divided by DIVIDER +1 (i.e., 1 to 16) [reset=0000b] A[7:4] Fosc frequency Frequency increases as setting value increases [reset=1100b]
0 1	B4 A[3:0]	1 *	0 *	1 *	1 *	0 A_3	1 A_2	0 A_1	0 A_0	Set Second Pre-charge Period	A[3:0] Set Second Pre-charge Period 0000b 0 DCLKS 0001b 1 DCLKS 0010b 2 DCLKS .... 0111 7 DCLKS [reset] .... 1111 15 DCLKS
0 1 1 1 1 1 1 1 1 1 1 1 1	B8 A1[3:0] : A7[3:0] A8[4:0] : A15[4:0] A16[5:0] : A31[5:0] A32[6:0] : A63[6:0]	1 * : * * : * * : * * : *	0 * : * * : * * : * A326 : A636	1 * : * * : * A165 : A315 A325 : A635	1 * : * A84 : A154 A164 : A314 A324 : A634	1 A13 : A73 A83 : A153 A163 : A313 A323 : A633	0 A12 : A72 A82 : A152 A162 : A312 A322 : A632	0 A11 : A71 A81 : A151 A161 : A311 A321 : A631	0 A10 : A70 A80 : A150 A160 : A310 A310 : A630	Set Gray Scale Table	These 63 parameters define Gray Scale (GS) Table in terms of Gamma Setting A1[3:0]: Gamma Setting for GS1, A2[3:0]: Gamma Setting for GS2, : A62[6:0]: Gamma Setting for GS62, A63[6:0]: Gamma Setting for GS63. **Note** (1) Input 1d for Gamma Setting 1, 2d for Gamma setting 2, ... ,127d for Gamma Setting127 (2) 0 < Setting of GS1 < Setting of GS2 < Setting of GS3..... Setting 62 < Setting 63 Refer to Section 8.8 for details.
0	B9	1	0	1	1	1	0	0	1	Enable Linear Gray Scale Table	Reset built in Linear Gray Scale table GS0 = Gamma Setting 0; GS1 = Gamma Setting 2 GS2 = Gamma Setting 4; GS3 = Gamma Setting 6; : GS31 = Gamma Setting 62 GS32 = Gamma Setting 65; GS33 = Gamma Setting 67; : GS62 = Gamma Setting 125; GS63 = Gamma Setting 127; Refer to Section 8.8 for details.

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1	BB A[5:1]	1 0	0 0	1 A_5	1 A_4	1 A_3	0 A_2	1 A_1	1 0	Set Pre-charge level	Set pre-charge voltage level. All three colors share the same pre-charge voltage. [RESET =3Eh] **A[5:1] Hex code pre-charge voltage** 00000 00h 0.10 x V_{CC} : : : 11111 3Eh 0.55 x V_{CC}
0 1	BE A[5:2]	1 0	0 0	1 A_5	1 A_4	1 A_3	1 A_2	1 0	0 0	Set V_{COMH}	Set COM deselect voltage level [reset =3Ch] A[5:2] = **A[5:2] Hex code V COMH** 0000 00h 0.51 x V_{CC} 0001 04h 0.53 x V_{CC} .. .. .. 1101 34h 0.79 x V_{CC} 1110 38h 0.81 x V_{CC} 1111 3Ch 0.84 x V_{CC}
0 1 1	C0	1 CBTR3 *	1 CBTR2 *	0 CBTR1 *	0 CBTR0 *	0 CATR3 CCTR3	0 CATR2 CCTR2	0 CATR1 CCTR1	0 CATR0 CCTR0	OTP Write	Program data from MCU to OTP for color coordinate tuning. Details refer to section 10.1.22 “OTP Write (C0h)”.
0	E2	1	1	1	0	0	0	1	0	Software Reset	Reset display circuit and stop Graphic Acceleration operations.
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation.
0 1	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A_2	0 1	1 0	Set Command Lock	A[2]: MCU protection status [RESET = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [RESET] A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.

Note

(1) “*” stands for “Don’t care”.

Graphic Acceleration Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1 1 1 1 1 1 1	21 A[7:0] B[7:0] C[7:0] D[7:0] E[5:0] F[5:0] G[5:0]	0 A_7 B_7 C_7 D_7 * * *	0 A_6 B_6 C_6 D_6 * * *	1 A_5 B_5 C_5 D_5 E_5 F_5 G_5	0 A_4 B_4 C_4 D_4 E_4 F_4 G_4	0 A_3 B_3 C_3 D_3 E_3 F_3 G_3	0 A_2 B_2 C_2 D_2 E_2 F_2 G_2	0 A_1 B_1 C_1 D_1 E_1 F_1 G_1	1 A_0 B_0 C_0 D_0 E_0 F_0 G_0	Draw Line	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End E[5:0] : Color C of the line F[5:0] : Color B of the line G[5:0] : Color A of the line **Note** (1) Please enter all 6 bits for Color setting: E[5:0], F[5:0] and G[5:0] , despite of the color format setting in command A0h
0 1 1 1 1 1 1 1 1 1	22 A[7:0] B[7:0] C[7:0] D[7:0] E[5:0] F[5:0] G[5:0] H[5:0] I[5:0] J[5:0]	0 A_7 B_7 C_7 D_7 * * * * * *	0 A_6 B_6 C_6 D_6 * * * * * *	1 A_5 B_5 C_5 D_5 E_5 F_5 G_5 H_5 I_5 J_5	0 A_4 B_4 C_4 D_4 E_4 F_4 G_4 H_4 I_4 J_4	0 A_3 B_3 C_3 D_3 E_3 F_3 G_3 H_3 I_3 J_3	0 A_2 B_2 C_2 D_2 E_2 F_2 G_2 H_2 I_2 J_2	1 A_1 B_1 C_1 D_1 E_1 F_1 G_1 H_1 I_1 J_1	0 A_0 B_0 C_0 D_0 E_0 F_0 G_0 H_0 I_0 J_0	Drawing Rectangle	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End E[5:0] : Color C of the line F[5:0] : Color B of the line G[5:0] : Color A of the line H[5:0] : Color C of the fill area I[5:0] : Color B of the fill area J[5:0] : Color A of the fill area **Note** (1) Please enter all 6 bits for Color setting: E[5:0], F[5:0] , G[5:0], H[5:0]. I[5:0] and J[5:0] , despite of the color format setting in command A0h (2) 0<A[7:0] < C[7:0] <159 (3) 0<B[7:0] < D[7:0]<131
0 1 1 1 1 1 1 1	23 A[7:0] B[7:0] C[7:0] D[7:0] E[7:0] F[7:0]	0 A_7 B_7 C_7 D_7 E_7 F_7	0 A_6 B_6 C_6 D_6 E_6 F_6	1 A_5 B_5 C_5 D_5 E_5 F_5	0 A_4 B_4 C_4 D_4 E_4 F_4	0 A_3 B_3 C_3 D_3 E_3 F_3	0 A_2 B_2 C_2 D_2 E_2 F_2	1 A_1 B_1 C_1 D_1 E_1 F_1	1 A_0 B_0 C_0 D_0 E_0 F_0	Copy	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End E[7:0] : Column Address of New Start F[7:0] : Row Address of New Start
0 1 1 1 1	24 A[7:0] B[7:0] C[7:0] D[7:0]	0 A_7 B_7 C_7 D_7	0 A_6 B_6 C_6 D_6	1 A_5 B_5 C_5 D_5	0 A_4 B_4 C_4 D_4	0 A_3 B_3 C_3 D_3	1 A_2 B_2 C_2 D_2	0 A_1 B_1 C_1 D_1	0 A_0 B_0 C_0 D_0	Dim Window	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End The effect of dim window: GS15~GS0 no change GS19~GS16 become GS4 GS23~GS20 become GS5 ... GS63~GS60 become GS15

Graphic Acceleration Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1 1 1 1	25 A[7:0] B[7:0] C[7:0] D[7:0]	0 A_7 B_7 C_7 D_7	0 A_6 B_6 C_6 D_6	1 A_5 B_5 C_5 D_5	0 A_4 B_4 C_4 D_4	0 A_3 B_3 C_3 D_3	1 A_2 B_2 C_2 D_2	0 A_1 B_1 C_1 D_1	1 A_0 B_0 C_0 D_0	Clear Window	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End
0 1	26 A[4:0]	0 *	0 *	1 *	0 A_4	0 0	1 0	1 0	0 A_0	Fill Enable / Disable	A[0] : 0b = Disable Fill for Draw Rectangle Command [reset] 1b = Enable Fill for Draw Rectangle Command A[3:1] : 000 (Reserved values) A[4] : 0b = Disable reverse copy (reset) 1b = Enable reverse during copy command.
0 1 1 1 1 1	27 A[7:0] B[7:0] C[7:0] D[7:0] E[1:0]	0 A_7 B_7 C_7 D_7 *	0 A_6 B_6 C_6 D_6 *	1 A_5 B_5 C_5 D_5 *	0 A_4 B_4 C_4 D_4 *	0 A_3 B_3 C_3 D_3 *	1 A_2 B_2 C_2 D_2 *	1 A_1 B_1 C_1 D_1 E_1	1 A_0 B_0 C_0 D_0 E_0	Continuous Horizontal & Vertical Scrolling Setup	A[7:0]: Set number of column as horizontal scroll offset Range: 0d-131d (no horizontal scroll if equals to 0 B[7:0]: Define start row address C[7:0]: Set number of rows to be horizontal scrolled B[7:0]+C[7:0] <=132 D[7:0]: Set number of row as vertical scroll offset Range: 0d-131d (no vertical scroll if equals to 0) E[1:0]: Set time interval between each scroll step 00b 3 frames 01b 5 frames 10b 50 frames 11b 100 frames **Note**: (1) Vertical scroll run with command A3h Set Vertical Scroll Area (2) The parameters should not be changed after scrolling is activated
0	2E	0	0	1	0	1	1	1	0	Deactivate horizontal scroll	Deactivate horizontal scrolling. **Note** (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

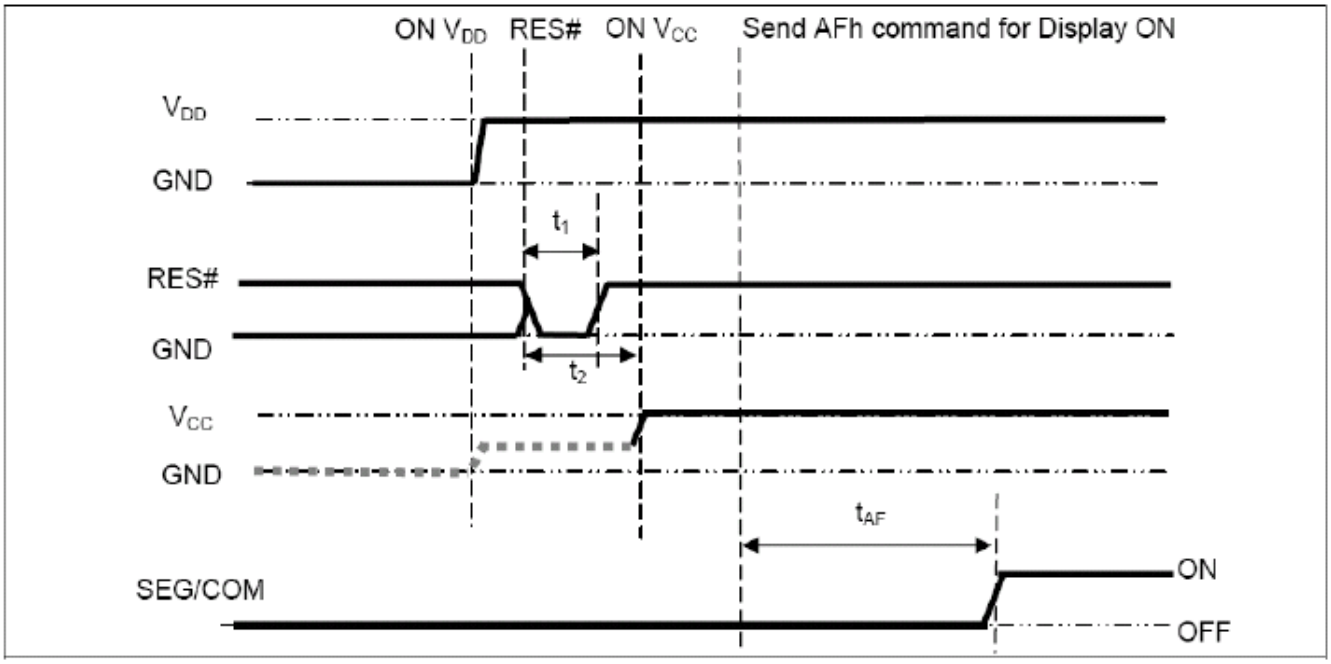
Graphic Acceleration Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	2F	0	0	1	0	1	1	1	1	Activate horizontal scroll	Activate horizontal scrolling. This command activates the scrolling function according to the setting done by command 27h Continuous Horizontal & Vertical Scrolling Setup
0 1 1	A3 A[7:0] B[7:0]	1 A_7 B_7	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	1 A_0 B_0	Set Vertical Scroll Area	A[7:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0] B[7:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 132] **Note** (1) A[7:0]+B[7:0] <= MUX ratio (2) B[7:0] <= MUX ratio (3) Set Display Start Line (A1h) must be set to 0 when using A3h command. (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 132d MUX display A[7:0] = 0, B[7:0]=132 : whole area scrolls A[7:0]= 0, B[7:0] < 132 : top area scrolls A[7:0] + B[7:0] < 132 : central area scrolls A[7:0] + B[7:0] = 132 : bottom area scrolls Refer to Figure 10-20 for details.

9.3 Power ON / OFF Sequence & Application Circuit

POWER ON / OFF SEQUENCE

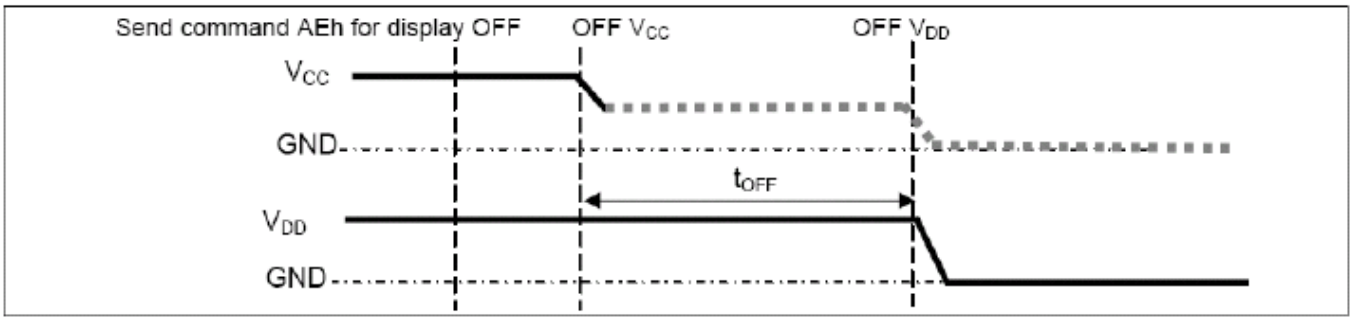
Power ON sequence:

1. Power ON V_{DD}.
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 100us(t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us(t_2).Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM wil be ON after 200ms(t_{AF}).



Power OFF sequence:

1. Send command AEh for display OFF.
2. Wait until panel discharges completely.
3. Power OFF V_{CC}. (1), (2)
4. Wait for t_{OFF}. Power OFF V_{DD}. (where Minimum t_{OFF}=0ms, Typical t_{OFF}=100ms)



Note:

(1) Since an ESD protection circuit is connected between VDD and VCC,VCC becomes lower than VDD whenever VDD is ON and VCC is OFF as shown in the dotted line of VCC in above figures.

(2)VCC should be disabled when it is OFF.

10. Quality Assurance

10.1 Inspection conditions

1. The inspection and meaurement are performed under the following conditions,
2. unless otherwise specified.
3. Temperature: 25±5°C
4. Humidity: 50±10%R.H.
5. Distance between the panel and eyes of the inspector≧30cm

10.2 Inspection Parameters

Severity	Inspection Item	Defect	Remark
Major Defect	1. Panel	(1) Non-displaying	
		(2) Line defects	
		(3) Malfunction	
		(4) Glass cracked	
	2. Film	(1) Film dimension out of specification	Can not be assembled
	3. Dimension	(1) Outline dimension out of specification	
Minor Defect	1. Panel	(1) Glass scratch	Appearance defect
		(2) Glass cutting NG	
		(3) Glass chip	
	2. Polarizer	(1) Polarizer scratch	
		(2) Stains on surface	
		(3) Polarizer bubbles	
	3. Displaying	(1) Dim spot、Bright spot、dust	
	4. Film	(1) Damage (2) Foreign material	

<table>
<tr><th>Description</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>1. Glass scratch</td><td>
<table>
<tr><th>Width (mm)
W</th><th>Length (mm)
L</th><th>number of pieces permitted</th></tr>
<tr><td>W≦0.03</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td>0.03＜ W≦0.05</td><td>L≦3</td><td>3</td></tr>
<tr><td>0.05＜ W</td><td>------</td><td>None</td></tr>
<tr><td>beyond A.A.</td><td>------</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2. Polarizer bubble</td><td>
<table>
<tr><th>Size</th><th>number of pieces permitted</th></tr>
<tr><td>Φ≦0.2</td><td>Ignore</td></tr>
<tr><td>0.2＜Φ≦0.5</td><td>2</td></tr>
<tr><td>0.5＜Φ</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>3. Dimming spot、
Lighting spot、
Dust</td><td>
<table>
<tr><th>average</th><th>number of</th></tr>
<tr><td>D ≦0.1</td><td>Ignore</td></tr>
<tr><td>0.1＜ D ≦0.15</td><td>2</td></tr>
<tr><td>0.15＜ D ≦0.2</td><td>1</td></tr>
<tr><td>0.2 ＜ D</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
D=(long diameter + short diameter)/2.
Pixel off is not allowed.
</td><td>Minor</td></tr>
</table>

10.3 WARRANTY POLICY

DISPLAY . Will provide one-year warranty for the products only if under specification operating conditions.

If there are functional defects found during the period of warranty, the defective products would be replaced on a one-to-one basis.

DISPLAY would not be responsible for any direct/indirect liabilities consequential to any parties.

10.4 MTBF

10.4.1 .MTBF based on specific test condition is 12K hours.

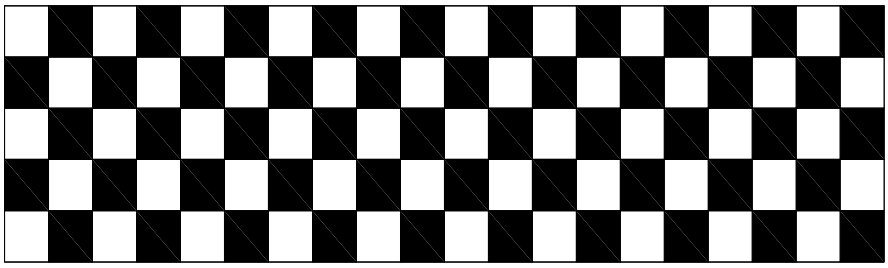
10.4.2 Test Condition:

10.4.2.1 Supply Voltage: Vcc=17V

10.4.2.2 Luminance: 80cd/m2

10.4.2.3 Operation temperature and humidity: 25°C and 50%RH

10.4.2.4 Run-Patterns:



10.4.3 Test Criteria:

Luminace has decayed to less than 50% of the initial measured luminance.

11.Reliability

■Content of Reliability Test

NO.	Items.	Specification	Applicable Standard
1	High temp. (Non-operation)	85°C, 240hrs	——
2	High temp. (Operation)	70°C, 120hrs	——
3	Low temp. (Operation)	-40°C, 120hrs	——
4	High temp. / High. humidity (Operation)	65°C, 90%RH, 96hrs	——
5	Thermal shock(Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 20 cycles.	——
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	——

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1 & 4 & 5.

Criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: >50% of initial value.
4. Current consumption : within ±50% of initial value.

Reliability Test

DISPLAY only guarantees the reliability of the panel under the test conditions and durations listed in the specification, and is not responsible for any test results that are conducted using more stringent conditions and/or with lengthened durations. Also, when the testing the panel in a chamber or oven, make sure they won't produce any condensation on the panel, especially on the electrical leads, before lighting on the panel to see if it passes the test. Also the panel should rest for about an hour at room temperature and pressure before the measurement, as indicated in the specification. Be aware that one should use fresh panel for each of the reliability test items listed in the specification, in other words, don't use the panels that were tested for subsequent tests.

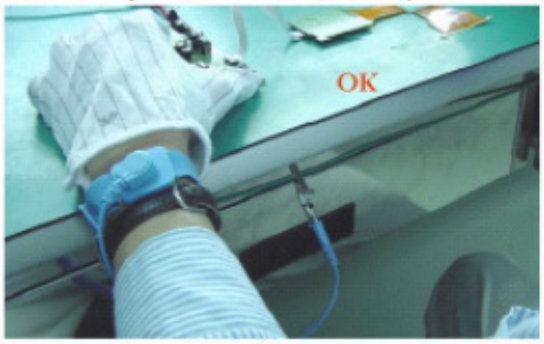
12. Precautions for Handling

12.1 When handling the module, wear powder-free antistatic rubber finger cots, and be careful not to bend and twist it.

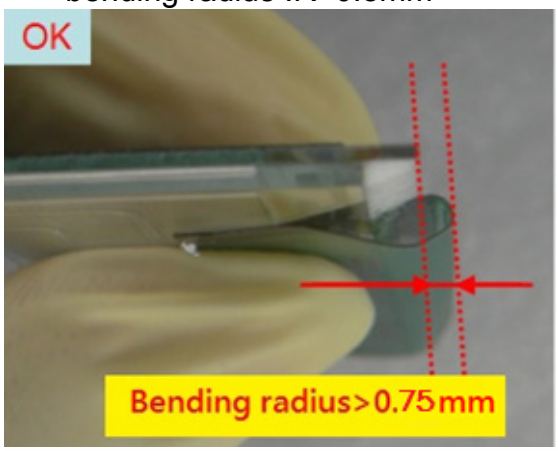
12.2 The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, or being dropped from a height.

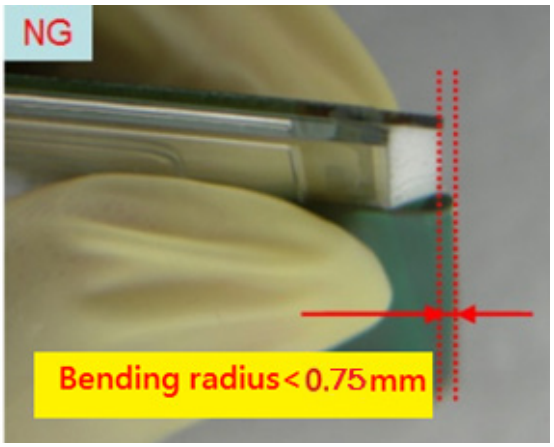
12.3 The OLED module is an electronic component and is subject to damage caused by Electro Static

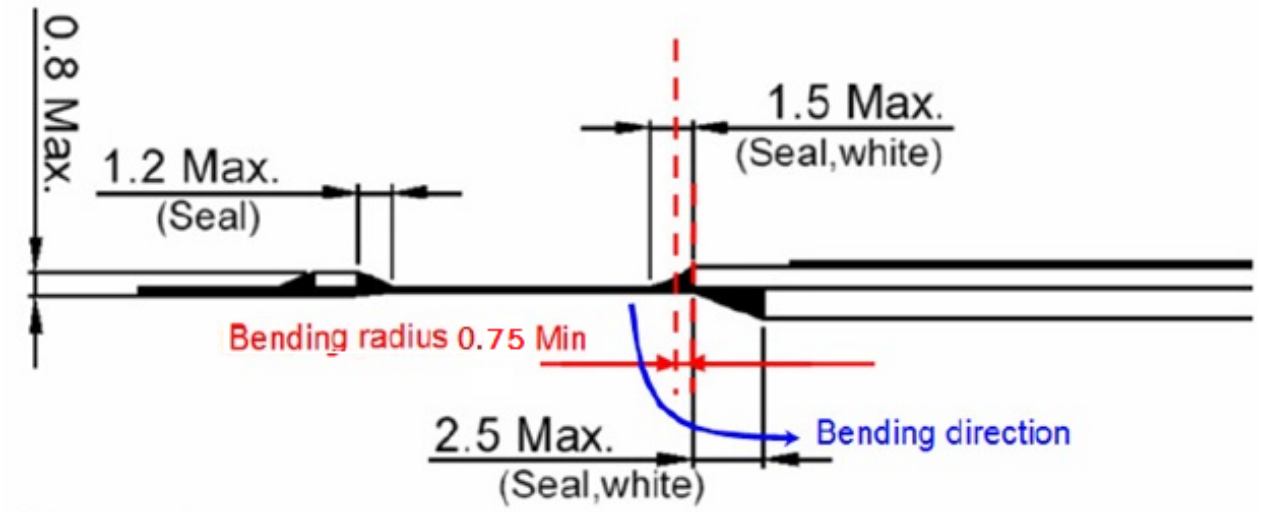
Discharge (ESD) and hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Also, ground the tools being used for panel assembly and make sure the working environment is not too dry to cause ESD problems. (See the photos below).



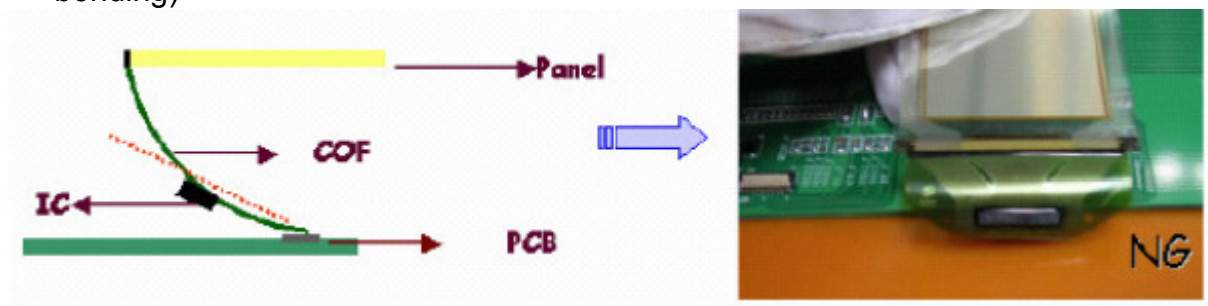
12.4 Please do not bend the film near the substrate glass.(this could cause film peeling and COF damage) and the peeling strength about 600g/cm, the bending <20times and the bending radius :R>0.8mm



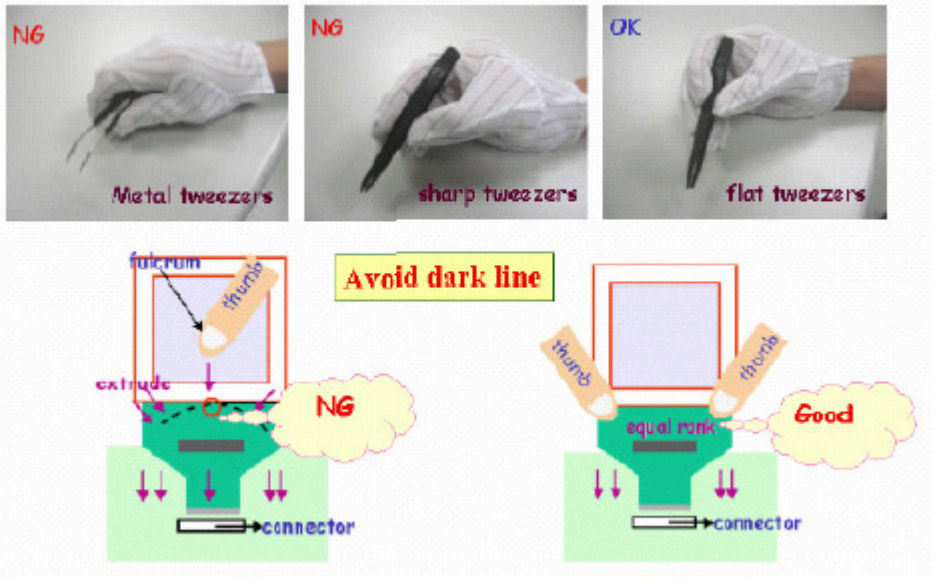




12.5 Avoid bending the film at IC bonding area.(>1.5mm)(this could damage the ILB bonding)



12.6 Use both thumbs to insert COF into the connector when assembling the panel. See the photo on the far right below for correct insertion of the film into the connector (one-handed insertion exerts uneven force on the film and could cause its breakage, photo on the left)



12.7 Do not wipe the pin of film with the dry or hard materials that will damage the surface. When cleaning the display surface, use soft cloth solvent and wipe gently (Recommend solvent: IPA, alcohol), and do not wipe the display with dry or hard materials that will damage the polarizer surface and do not use the solvent like: Water, Acetone, Aromatic

13. Precautions for Electrical

13.1. Design using the settings in the specification

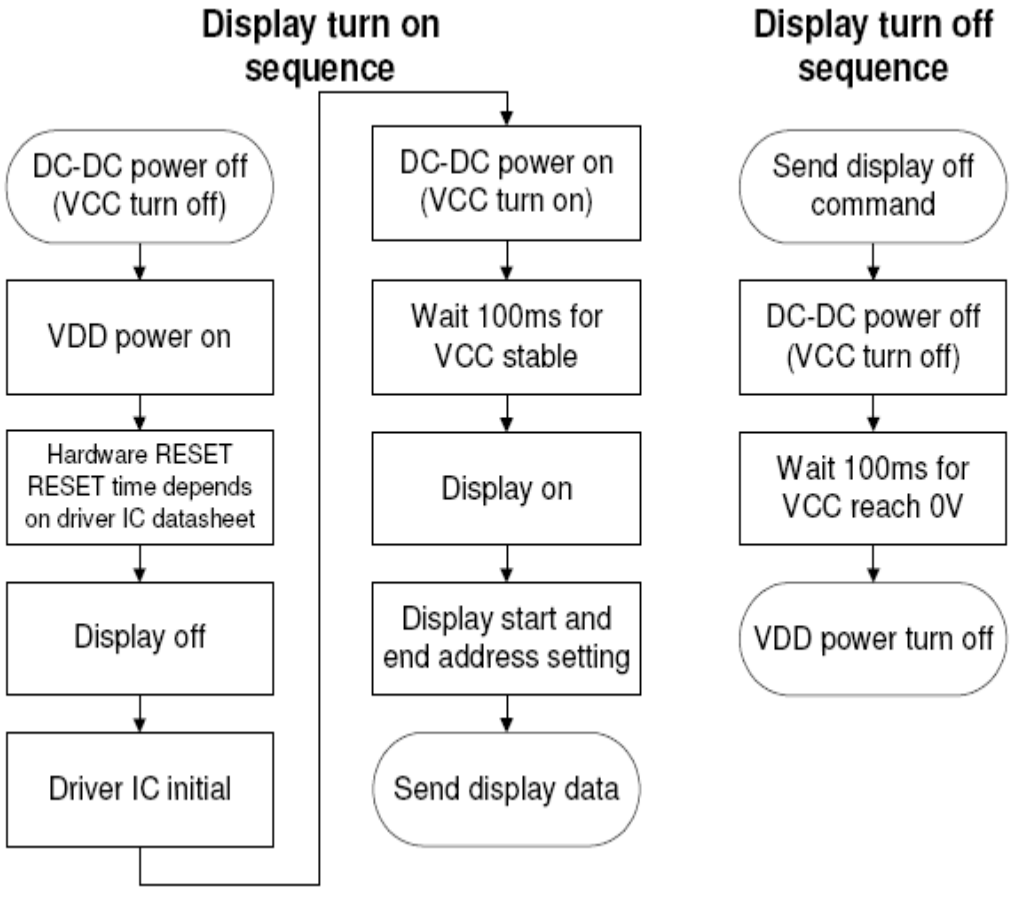
It is extremely important to design and operate the panel using the settings listed in the specification. This includes voltage, current, frame rate, duty cycle... etc. Operation of the OLED outside the specified range in the specification should be entirely avoided to ensure proper operation of the OLED.

13.2. Maximum Ratings

To ensure proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.

13.3 Power on/off procedure

Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, could cause OLED panel malfunctioning.



13.4 Power savings

To save power consumption of the OLED, one can use partial display or sleep mode when the panel is not fully activated. Also, if possible, make maximum use of black background to save power. The OLED is a self-luminous device, and a particular pixel cluster or image can be lit on via software control, so power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright Mode, Normal Operation Mode, and Sleeping Mode.

The power consumption is almost in direct proportion to the brightness of the panel, and also in direct proportion to the number of pixels lit on the panel, so the customer can save the power by the use of black background and Sleeping Mode. One benefit from using these design schemes is the extension of the OLED lifetime.

13.5 Residual Image (Image Sticking)

The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. The time when image sticking happens depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following three strategies to minimize image sticking

13.5.1 Employ image scrolling or animation to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.

13.5.2 Minimize the use of all-pixels-on or full white background in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays

13.5.3 If in the reliability test when a static logo is used, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns

14. Precautions for Storage

Although the storage conditions and guarantee period are indicated in the specification, it is advisable to store the packed cartons or packages at 23°C±5°C,55%±10%RH. Do not store the OLED module under direct sunlight or UV light and for best panel performance.

※The OLED module would be decayed due to humidity, please keep the environment dry whenever in the operating or storage.	
OK	NG