

Display Elektronik GmbH

DATA SHEET

TFT MODULE

**DEM 240320U VMH-PW-N
(C-TOUCH)**

1,77" TFT + CTP

Version: 0

29.09.2025

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1. Basic Specifications*** Description**

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit, capacitance touch panel, Backlight unit. The resolution of a 1.77" TFT-LCD contains 240x320 pixels, and can display up to 65k/262k colors.

1.1 TFT Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display Area(AA)	26.64 x 35.52 (1.77 Inch)	mm	-
Driver Element	TFT Active Matrix	-	-
Display Colors	65k/262k	colors	-
Number of Pixels	240 x (RGB) x 320	dots	-
Pixel Arrangement	RGB Vertical Stripe	-	-
Pixel Pitch	0.111 x 0.111	mm	-
Viewing Angle	Free	o'clock	-
Controller IC	ST7789V (Sitronix)	-	-
Display Mode	IPS, Transmissive / Normally Black	-	-
LCM Interface	8/9/16/18Bit-MCU 3/4SPI+16/18Bit-RGB 3-Line/4-Line Serial Interface	-	-
Operating Temperature	-29°C to +70°C	°C	-
Storage Temperature	-30°C to +80°C	°C	-
Module Bonding Technology	Use Tape bonding between LCM and CTP	-	-

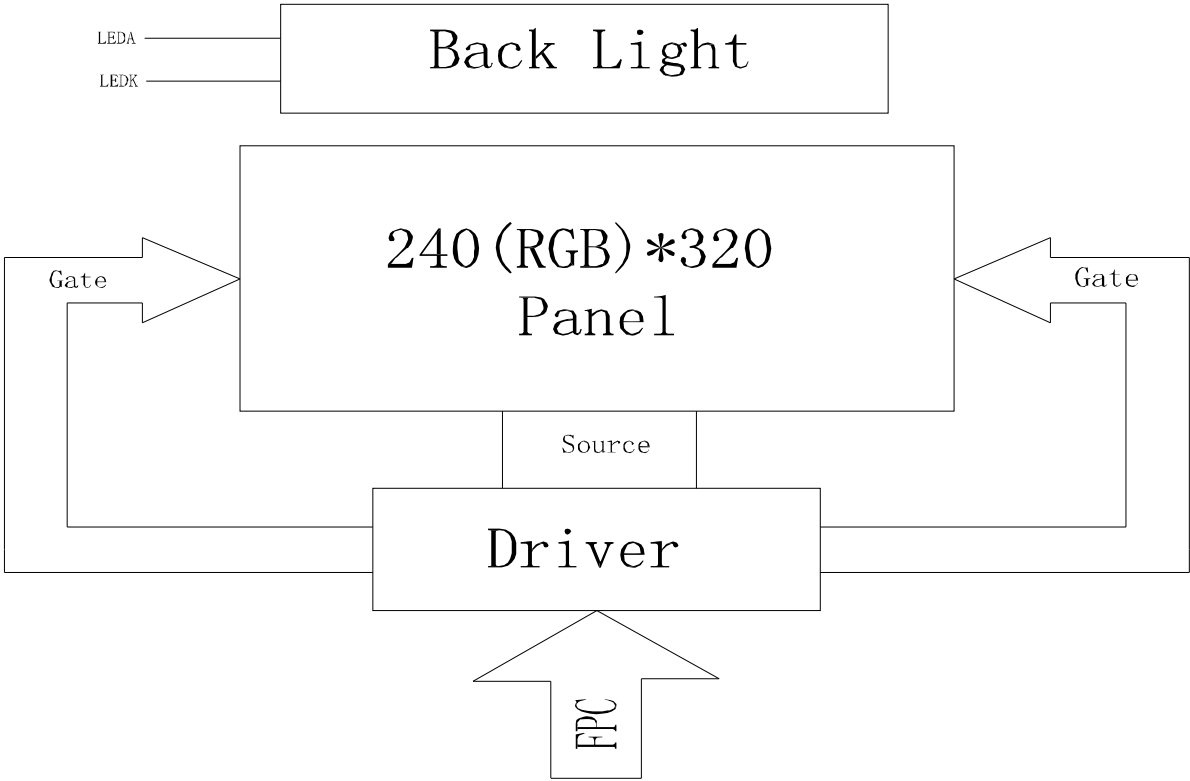
1.2 CTP Features

General Information Items	Specification	Unit	Note
	Main Panel		
Resolution	240 x 320(V)	-	-
Structure	G+G	-	-
Controller IC	FT5436 (Focaltech)	-	-
Interface	I2C	-	-
Slave Address	0x38(7bit) / 8bit:0x70(Write) 0x71(Read)	-	-
Touch Mode	Single Point and Gestures	-	-

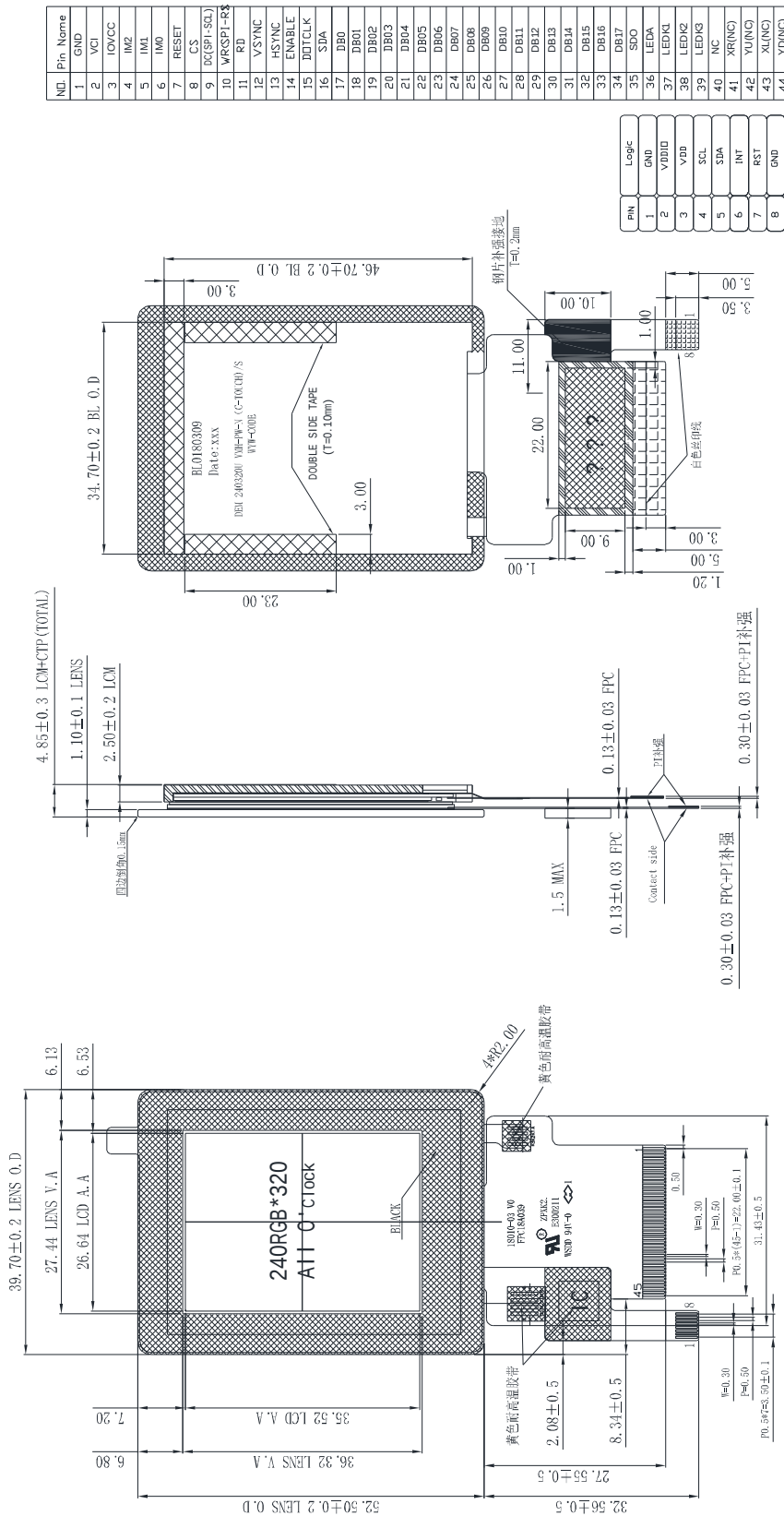
1.3 Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	-	39.70	-	mm	-
	Vertical(V)	-	52.50	-	mm	-
	Depth(D)	-	4.85	-	mm	-
Weight		-	t.b.d.	-	g	-

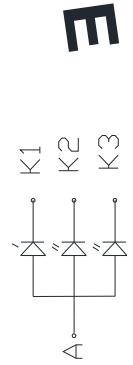
2. Block Diagram



3. Outline Dimension



NO.	Pin	IOVCC	Interface type	DB Pin	IOVCC
0	0	0	DBI Typ. 8-bit interface	D07-D80	
1	1	1	DBI Typ. 8-bit interface	D815-D80	
2	2	2	DBI Typ. 8-bit interface	D88-D80	
3	3	3	DBI Typ. 10-bit interface	D817-D80	
4	4	4	3-Byte 8-BIT data serial interface	S0A SCL CS	
5	5	5	4-Byte 8-BIT data serial interface	S0A SCL CS RS	



- NOTES:
1. DISPLAY TYPE: 1.77", TFT-LCD
 2. DISPLAY MODE: T/N NORMALLY BLACK
 3. VIEWING DIRECTION: ALL
 4. DRIVER IC: ST7789V (COG)
 5. CTP IC: FT5436
 6. VCI: 2.8~3.3V(TYP),IOVCC=1.8V~3.3V
 7. OPERATING TEMP: -20°C TO 70°C
 8. STORAGE TEMP: -30°C TO 80°C
 9. BACK LIGHT: LED WHITE, 3 LED, 60mA, 3.2±0.3V
 10. RoHS COMPLIANT.

4. Input Terminal Pin Assignment

4.1 TFT PIN Definition

NO	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VCI/VCC	Supply voltage (3.3V).	P
3	IOVCC	Supply voltage (1.65-3.3V).	P
4	IM2	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. Fix this pin at IOVCC and GND.	I
5	IM1		I
6	IM0		I
7	RESET	This signal will reset the device and must be applied to properly initialize the chip.	I
8	CS	Chip select input pin ("Low" enable). fix this pin at IOVCC or GND when not in use.	I
9	DC(SPI-SCL)	- Display data/command selection pin in parallel interface. - This pin is used to be serial interface clock. DC='1': display data or parameter. DC='0': command data. - If not used, please fix this pin at IOVCC or DGND.	I
10	WR(SPI-RS)	- Write enable in MCU parallel interface. - Display data/command selection pin in 4-line serial interface. - Second Data lane in 2 data lane serial interface. - If not used, please fix this pin at IOVCC or DGND.	I
11	RD	Serves as a read signal and MCU read data at the rising edge. Fix this pin at IOVCC or GND when not in use.	I
12	VSYNC	Frame synchronous signal. Low active. Connect to I GND when DPI is not selected.	I
13	HSYNC	Line synchronous signal. Low active. Connect to GND when DPI is not selected.	I
14	ENABLE	Data enable signal in DPI operation. Low: Select (Accessible) High: Not select (Inaccessible) Connect to GND when DPI is not selected.	I
15	DOTCLK	Pixel clock signal. The data input timing is set on the rising edge. Connect to GND when DPI is not selected.	I
16	SDA	Serial data input/output pin in DBI Type C operation.	I

17~34	DB0~DB17	Data bus. Connect to GND when is not used.	P
35	SDO	SPI interface output pin. The data is output on the falling edge of the SCL signal. If not used, let this pin open.	O
36	LEDA	Anode pin of backlight.	P
37	LEDK1	Cathode pin of backlight.	P
38	LEDK2	Cathode pin of backlight.	P
39	LEDK3	Cathode pin of backlight.	P
40	NC	NC	
41	XR	Touch panel Right Glass Terminal	A/D
42	YU	Touch panel Top Film Terminal	A/D
43	XL	Touch panel LIFT Glass Terminal	A/D
44	YD	Touch panel Bottom Film Terminal	A/D
45	GND	Ground.	P

4.2 CTP PIN Define

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VDDIO	I/O power supply voltage.	P
3	VDD	Supply voltage.	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P

5. LCD Optical Characteristics

5.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	$\Theta=0$ Normal Viewing Angle	500	600	-	-	-
Response Time	Rising	T _R		--	20	45	msec	-
	Falling	T _F		--	35	50		
Color Gamut		S(%)	-	--	49.3	--	%	-
Color Filter Chromaticity	White	W _X	-	0.260	0.300	0.340	-	-
		W _Y	-	0.280	0.320	0.360		
	Red	R _X	-	0.609	0.629	0.649		
		R _Y	-	0.307	0.327	0.347		
	Green	G _X	-	0.292	0.312	0.332		
		G _Y	-	0.535	0.555	0.575		
	Blue	B _X	-	0.144	0.164	0.184		
		B _Y	-	0.149	0.169	0.189		
Viewing Angle	Hor.	Θ_L	CR>10	60	85	--	-	-
		Θ_R		60	85	--		
	Ver.	Θ_U		60	85	--		
		Θ_D		60	85	--		
Option View Direction		Free						

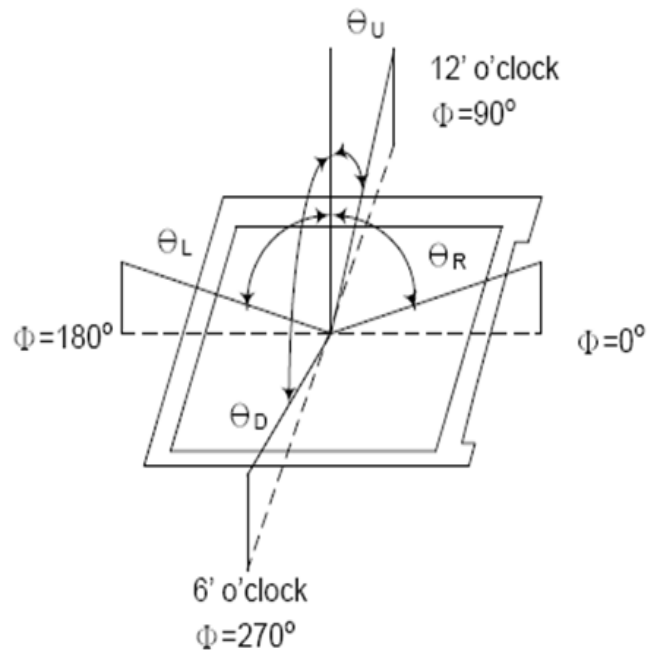
5.2 Measuring Condition

- Measuring surrounding: dark room
- Ambient temperature: 25°C±2°C
- 15min. warm-up time

5.3 Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

Note (1) Definition of Viewing Angle:



Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

6. Electrical Characteristics

6.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VCI	-0.3	4.6	V
Digital Interface Supply Voltage	IOVCC	-0.3	4.6	V
Operating Temperature	T _{OP}	-20	+70	°C
Storage Temperature	T _{ST}	-30	+80	°C

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

6.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.4	3.3	3.6	V	-
Digital Interface Supply Voltage	IOVCC	1.65	1.8	3.3	V	-
Normal Mode Current Consumption	IDD	--	7	--	mA	-
Level Input Voltage	V _{IH}	0.7IOVCC	-	IOVCC	V	-
	V _{IL}	GND	-	0.3IOVCC	V	-
Level Output Voltage	V _{OH}	0.8IOVCC	-	IOVCC	V	-
	V _{OL}	GND	-	0.2IOVCC	V	-

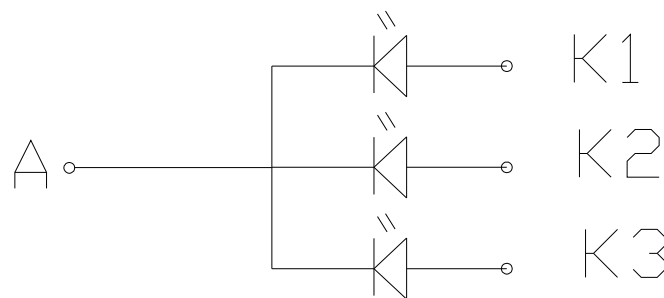
6.3 LED Backlight Characteristics

The Backlight System is edge-lighting type with 3 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	45	60	--	mA	--
Forward Voltage	V_F	--	3.2	--	V	--
LCM Luminance	L_v	200	250	--	cd/m ²	Note3
LED Lifetime	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

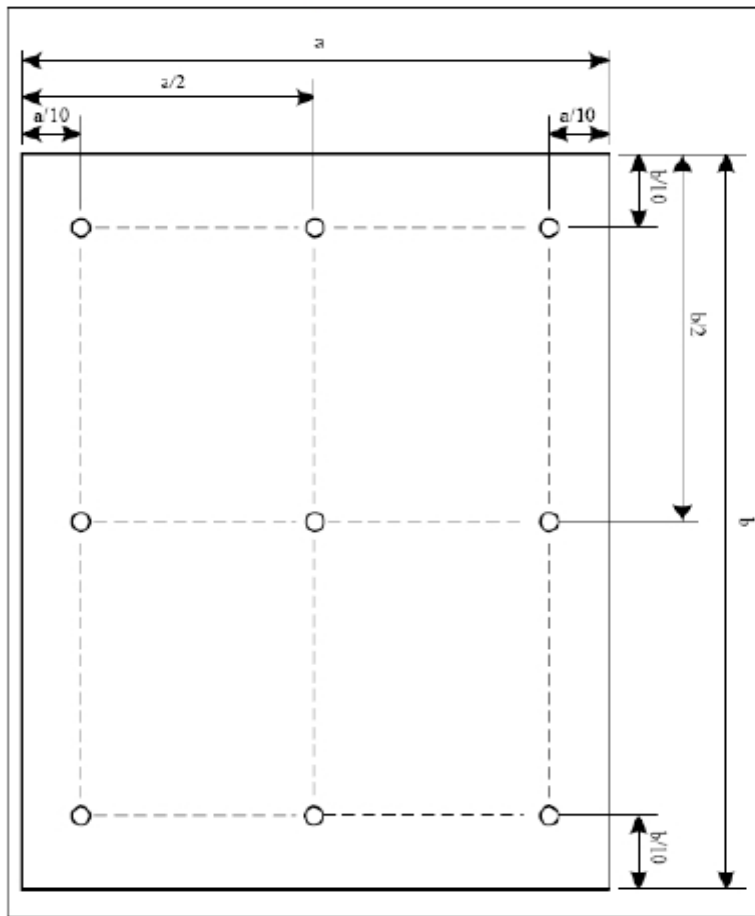
Note (1) LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: $T_a=25^{\circ}\text{C}\pm 3^{\circ}\text{C}$, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The “LED lifetime” is defined as the module brightness decrease to 50% original brightness at $T_a=25^{\circ}\text{C}$ and $I_L=60\text{mA}$. The LED lifetime could be decreased if operating I_L is larger than 60mA. The constant current driving method is suggested.



LED CIRCUIT DIAGRAM

NOTE 3: Luminance Uniformity of these 9 points is defined as below:

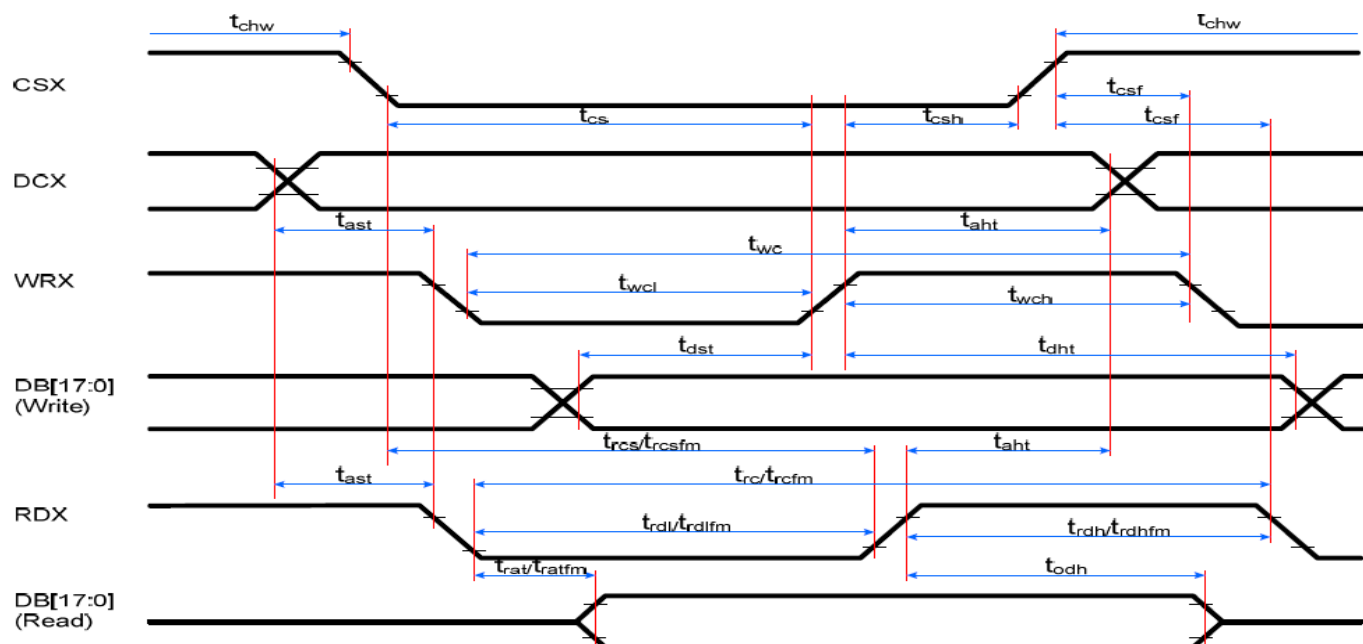


$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

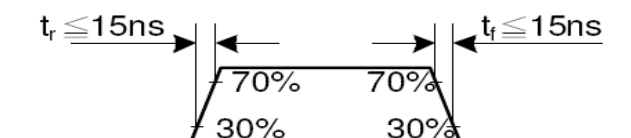
7. AC Characteristic

7.1 Display Parallel 8/16-Bit Interface Timing Characteristics (8080 System)

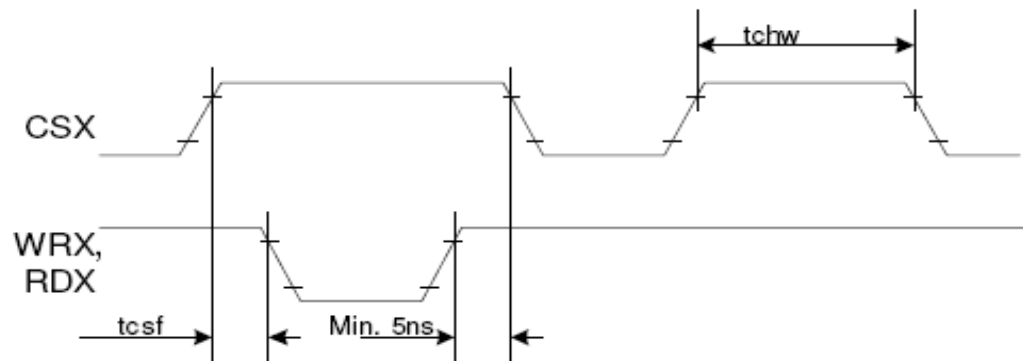


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t _{ast}	Address setup time	0	-	ns	
	t _{ahh}	Address hold time (Write/Read)	10	-	ns	
CSX	t _{chw}	CSX "H" pulse width	0	-	ns	
	t _{cs}	Chip Select setup time (Write)	15	-	ns	
	t _{rcs}	Chip Select setup time (Read ID)	45	-	ns	
	t _{trcsfm}	Chip Select setup time (Read FM)	355	-	ns	
	t _{csf}	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	t _{wc}	Write cycle	66	-	ns	
	t _{wrh}	Write Control pulse H duration	15	-	ns	
	t _{wrl}	Write Control pulse L duration	15	-	ns	
RDX (FM)	t _{trcfm}	Read Cycle (FM)	450	-	ns	
	t _{trdhfm}	Read Control H duration (FM)	90	-	ns	
	t _{trdlfm}	Read Control L duration (FM)	355	-	ns	
RDX (ID)	t _{trc}	Read cycle (ID)	160	-	ns	
	t _{trdh}	Read Control pulse H duration	90	-	ns	
	t _{trdl}	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	t _{dst}	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t _{dht}	Write data hold time	10	-	ns	
	t _{rat}	Read access time	-	40	ns	
	t _{ratfm}	Read access time	-	340	ns	
	t _{rod}	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 2.8V, VCI=2.6V to 3.3V, GND=0V

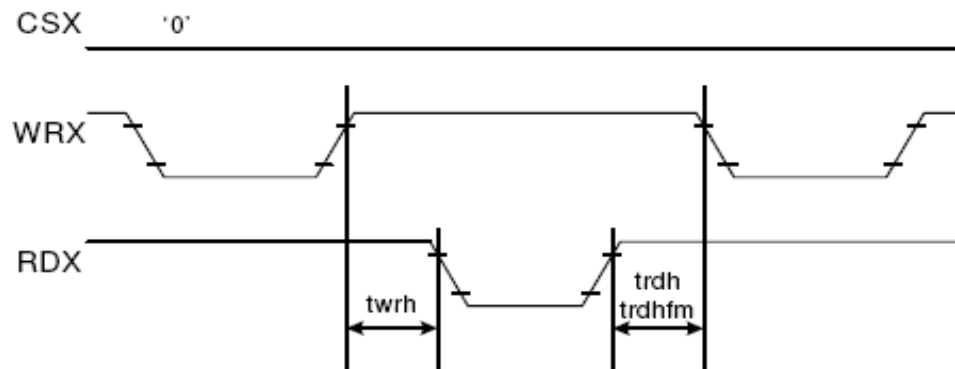


CSX timings :



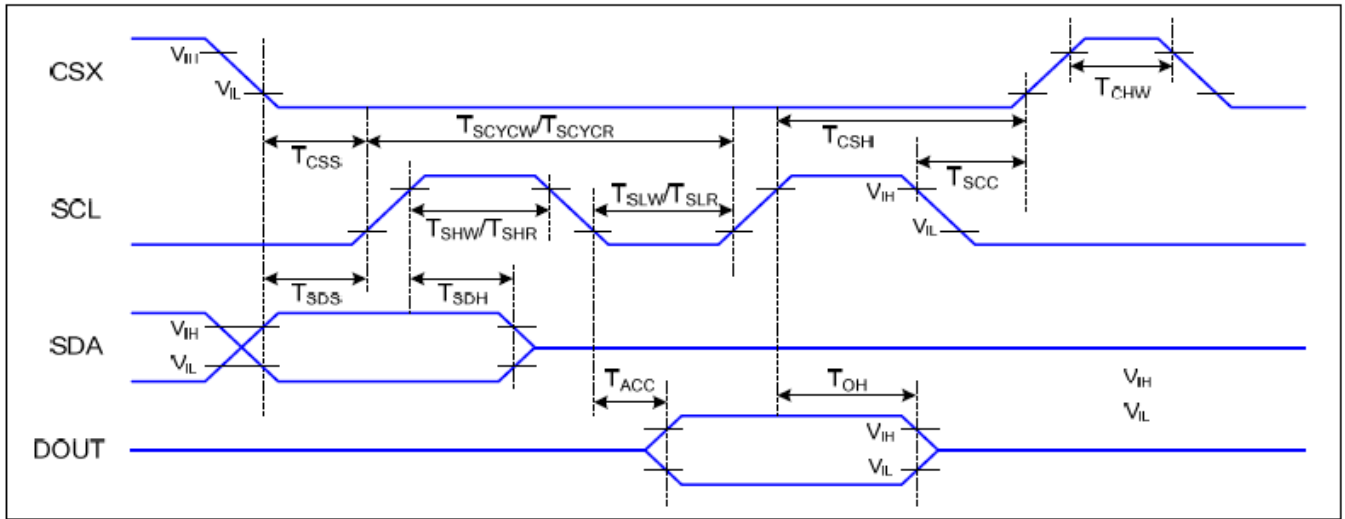
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

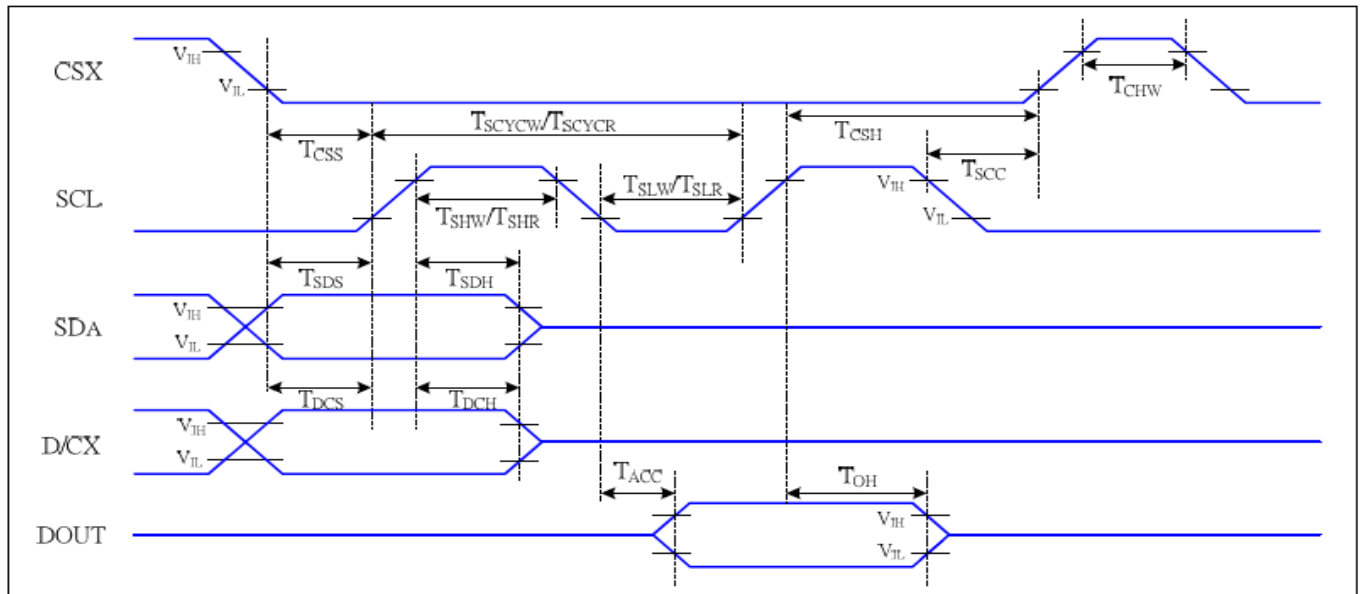
7.2 Display Serial Interface Timing Characteristics (3-Line SPI System)



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T _{CS}	Chip select setup time (write)	15		ns	
	T _{CS}	Chip select hold time (write)	15		ns	
	T _{CS}	Chip select setup time (read)	60		ns	
	T _{SC}	Chip select hold time (read)	65		ns	
	T _{CHW}	Chip select "H" pulse width	40		ns	
SCL	T _{SCYC}	Serial clock cycle (Write)	66		ns	
	T _{SHW}	SCL "H" pulse width (Write)	15		ns	
	T _{SLW}	SCL "L" pulse width (Write)	15		ns	
	T _{SCYC}	Serial clock cycle (Read)	150		ns	
	T _{SHR}	SCL "H" pulse width (Read)	60		ns	
	T _{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T _{SDS}	Data setup time	10		ns	
	T _{SDH}	Data hold time	10		ns	
DOUT	T _{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T _{OH}	Output disable time	15	50	ns	For minimum CL=8pF

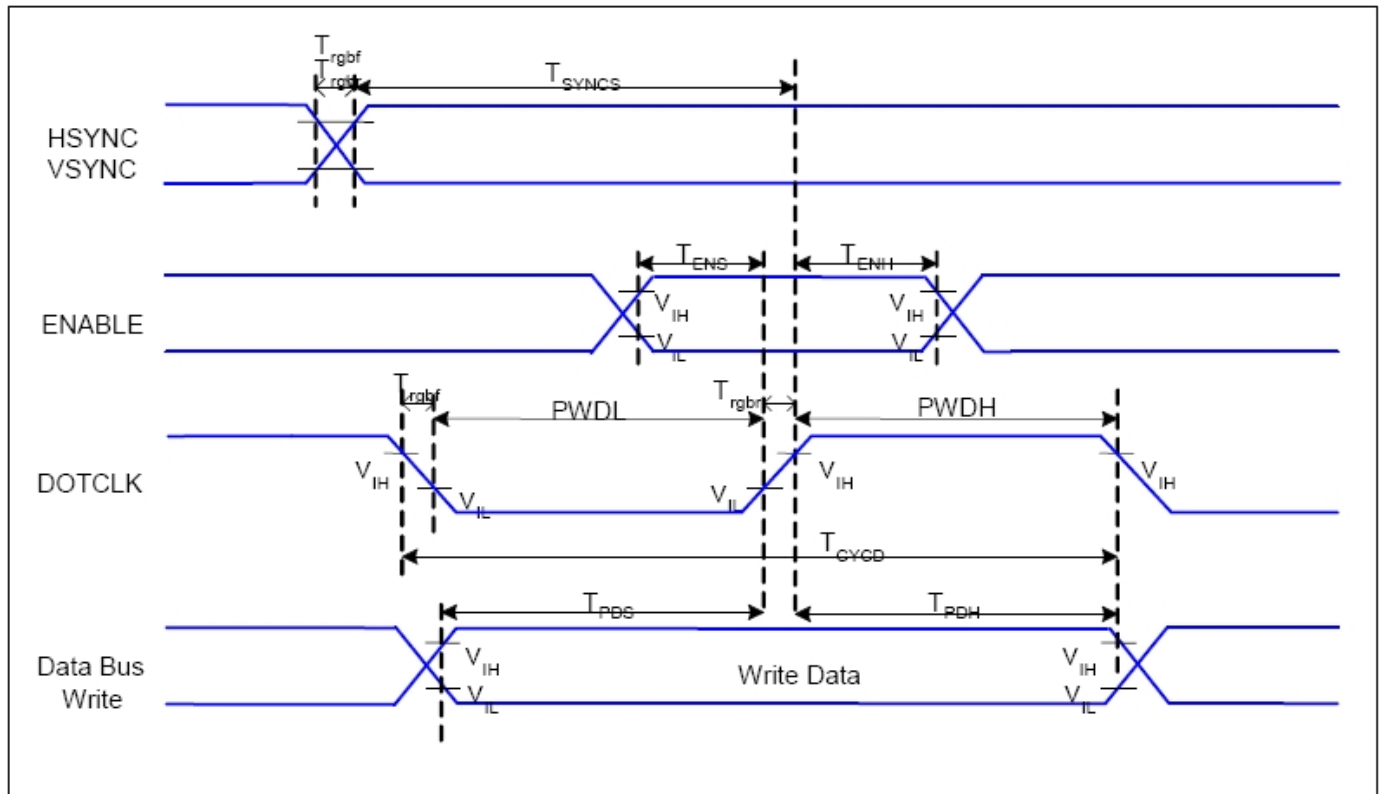
7.3 Display Serial Interface Timing Characteristics (4-Line SPI System)



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 °C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

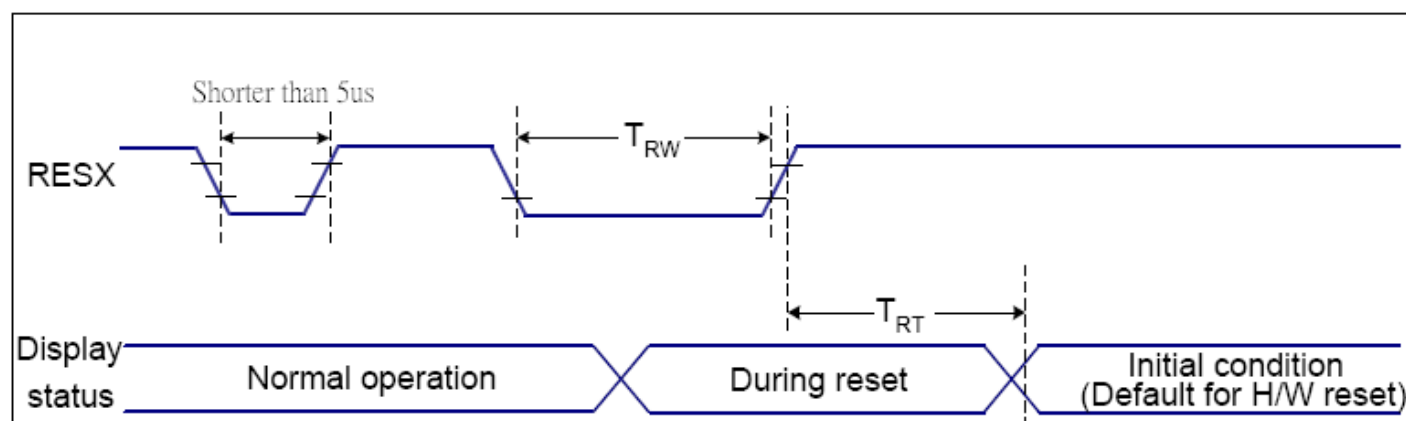
7.4 Parallel RGB Interface Timing Characteristics



$V_{DDI}=1.65$ to $3.3V$, $V_{DD}=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a=-30 \sim 70^{\circ}C$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYSNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	$PWDH$	DOTCLK High-level Pulse Width	60	-	ns	
	$PWDL$	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	T_{rghr}, T_{rgbf}	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

7.5 Reset Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 °C

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

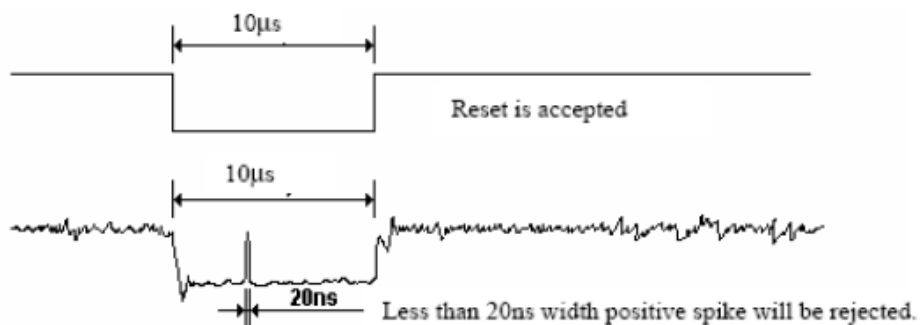
Notes:

- The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
- Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

- During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

- Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. CTP Specification

8.1 Electrical Characteristics

8.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	2.7	3.6	V	--
Operating Temperature	T _{OP}	-40	+85	°C	--
Storage Temperature	T _{ST}	-55	+150	°C	--

8.1.2 DC Electrical Characteristics (Ta=25°C)

(Ambient Temperature: 25°C, AVDD=2.8V, VDDIO=1.8V or VDDIO=AVDD)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	VIH	V		0.7 x IOVCC	--	IOVCC	
Input low -level voltage	VIL	V		-0.3	--	0.3 x IOVCC	
Output high -level voltage	VOH	V	IOH=3mA	0.7 x IOVCC	--	--	
Output low -level voltage	VOL	V	IOL=4.5mA	--	--	0.3 x IOVCC	
I/O leakage current	ILI	uA	Vin=0~VDD3	-1	--	1	
Current consumption (Normal operation mode)	Iopr	mA	VDD3 = 3V Ta=25°C	--	11	--	
Current consumption (Monitor mode)	Imon	mA	VDD3 = 3V Ta=25°C	--	0.43	--	
Current consumption (Sleep mode)	Islp	uA	VDD3 = 3V Ta=25°C	--	42	--	
Step-up output voltage	VDD5	V	VDD3= 2.8V		0.25		
Step-up output voltage	VDD10	V	VDD3= 2.8V		0.5		
Power Supply voltage	VDD3	V		2.7	--	3.6	

Notes: This sample data is intended for design guidance only. Values shown are typical for a 15Tx × 24Rx sensor configured at 80 Hz report rate. Actual current will depend on the particular sensor design and firmware options.

8.1.3 AC Characteristics

AC Characteristics of Oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDD3 = 2.8V; Ta=25°C	49	50	51	

Table 3-3 AC Characteristics of TX & RX

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
TX acceptable clock	ftx		50	150	400	KHz	
TX output rise time	Ttxr		--	210	--	nS	
TX output fall time	Ttxf		--	210	--	nS	
RX input voltage	Trxi		1.2	--	1.6	V	

8.2 POWER ON/Reset Sequence

Reset should be pulled down to be low before powering on and powering down. I2C shouldn't be used by other devices during Reset time after VDD powering on (Trtp). INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Tpdtt is more than 1ms.

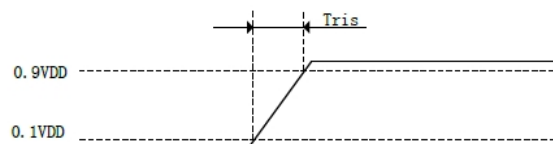


Figure 3-3 Power on time

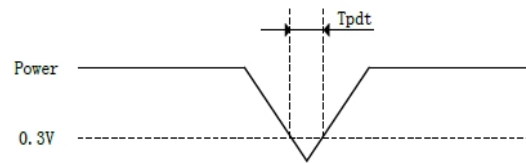


Figure 3-4 Power Cycle requirement

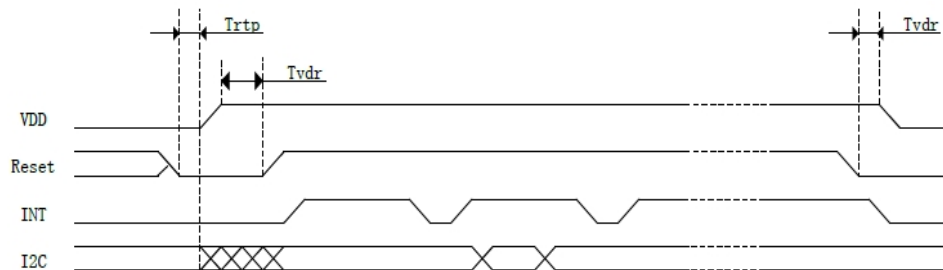


Figure 3-5 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

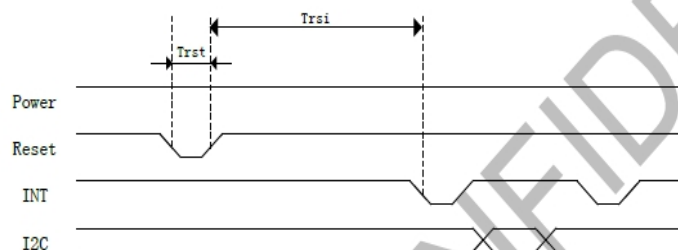


Table 3-5 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	5	--	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	--	200	ms
Trst	Reset time	1	--	ms

9. LCD Module Out-Going Quality Level

9.1 VISUAL & FUNCTION INSPECTION STANDARD

9.1.1 Inspection Conditions

Inspection performed under the following conditions is recommended.

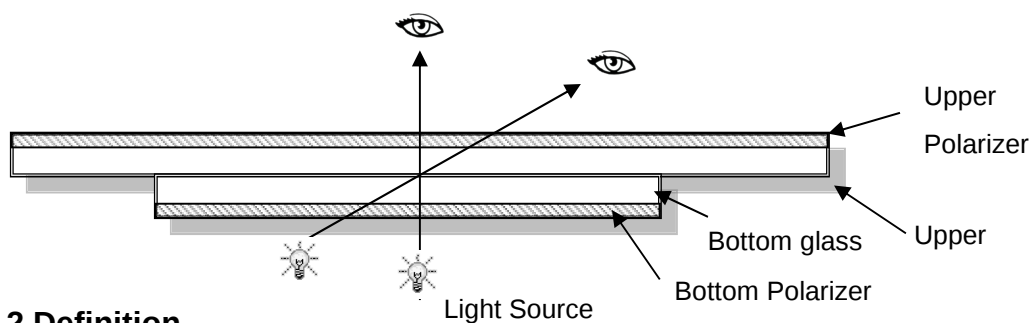
Temperature: $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$

Humidity: $65\%\text{RH} \pm 10\%\text{RH}$

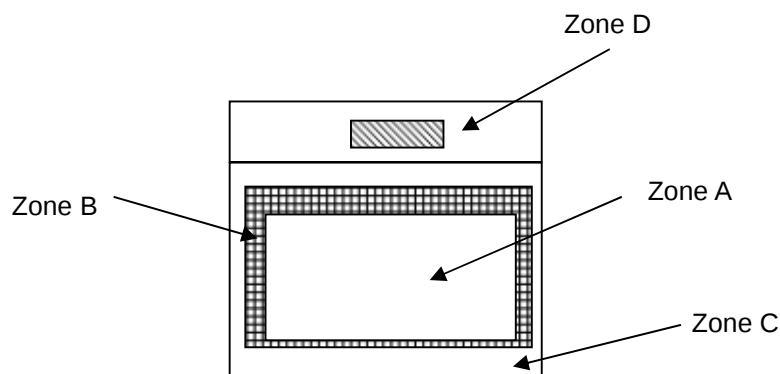
Viewing Angle: Normal Viewing Angle.

Illumination: Single fluorescent Lamp (300 to 700Lux)

Viewing distance: 30-50cm



9.1.2 Definition



Zone A: Effective Viewing Area (Character or Digit can be seen)

Zone B: Viewing Area except Zone A

Zone C: Outside (Zone A+Zone B) which cannot be seen after assembly by customer.)

Zone D: IC Bonding Area

Note: As a general rule, visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

9.1.3 Sampling Plan

According to GB/T 2828-2003; Normal Inspection, Class II

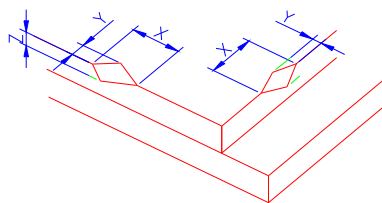
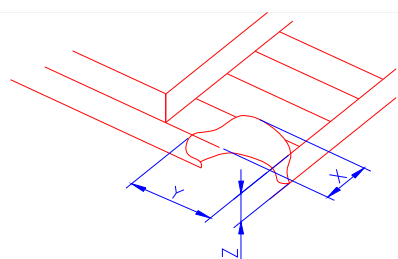
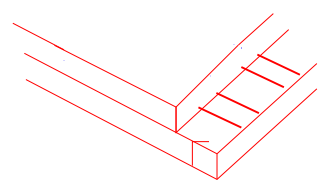
AQL:

Major Defect	Minor Defect
0.65	1.5

LCD: Liquid Crystal Display, TP: Touch Panel, LCM: Liquid Crystal Module

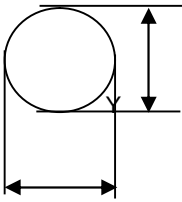
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

9.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of ITO, T: Height of LCD	(1) The edge of LCD broken	 <table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2)LCD corner broken	 <table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) LCD crack	 Crack Not allowed							

2.0

Spot defect



X

$$\Phi = (X+Y)/2$$

① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.10$	Ignore		Ignore
$0.10 < \Phi \leq 0.20$	3(distance $\geq 10\text{mm}$)		
$0.20 < \Phi \leq 0.25$	2		
$\Phi > 0.3$	0		

② Dim spot (LCD/TP/Polarizer dim dot, light leakage、 dark spot)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.1$	Ignore		Ignore
$0.10 < \Phi \leq 0.20$	3(distance $\geq 10\text{mm}$)		
$0.20 < \Phi \leq 0.25$	2		
$\Phi > 0.3$	0		

③ Polarizer accidented spot

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		Ignore
$0.3 < \Phi \leq 0.5$	2(distance $\geq 10\text{mm}$)		
$\Phi > 0.5$	0		

④ Pixel bad points (light dot, Dim dot, color dot)

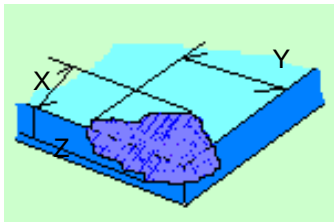
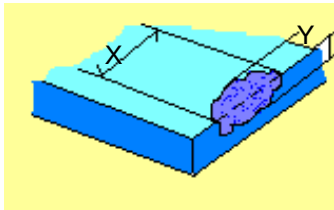
Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.1$	Ignore	Ignore	
$0.15 < \Phi \leq 0.2$	2(distance $\geq 10\text{mm}$)		
$\Phi > 0.2$	0		

⑤ Polarizer Bubble

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		Ignore
$0.3 < \Phi \leq 0.4$	3(distance $\geq 10\text{ m}$)		
$0.4 < \Phi \leq 0.5$	2		
$\Phi > 0.5$	0		

3.0	Line defect (LCD/TP /Polarizer backlight black/white line, scratch, stain)	Width(mm)	Length(mm)	Acceptable Qty		
				A	B	C
		$\Phi\leq0.03$	Ignore	Ignore		Ignore
		$0.03<W\leq0.04$	$L\leq3.0$	$N\leq2$		
		$0.04<W\leq0.05$	$L\leq2.0$	$N\leq1$		
$0.05<W$	Define as spot defect					
4.0	Electronic Components SMT	Not allow missing parts, solderless connection, cold solder joint, mismatch, The positive and negative polarity opposite				
5.0	Display color& Brightness	Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.				
6.0	LCD Mura	By 5% ND filter invisible.				

7.0	CTP Related	CTP Cover sensor accidented black/white spot	<table><tr><th rowspan="2">Size Φ(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi \leq 0.1$</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>$0.1 < \Phi \leq 0.2$</td><td colspan="2">3 (distance $\geq 10\text{mm}$)</td></tr><tr><td>$0.20 < \Phi \leq 0.25$</td><td colspan="2">2</td></tr><tr><td>$\Phi > 0.3$</td><td colspan="2">0</td></tr></table>				Size Φ (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.1$	Ignore		Ignore	$0.1 < \Phi \leq 0.2$	3 (distance $\geq 10\text{mm}$)		$0.20 < \Phi \leq 0.25$	2		$\Phi > 0.3$	0								
			Size Φ (mm)	Acceptable Qty																													
				A	B	C																											
			$\Phi \leq 0.1$	Ignore		Ignore																											
			$0.1 < \Phi \leq 0.2$	3 (distance $\geq 10\text{mm}$)																													
			$0.20 < \Phi \leq 0.25$	2																													
		$\Phi > 0.3$	0																														
		CTP Cover scratch	<table><tr><th rowspan="2">Width(mm)</th><th rowspan="2">Ignore(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi \leq 0.05$</td><td>Ignore</td><td colspan="3">Ignore</td></tr><tr><td>$0.05 < W \leq 0.06$</td><td>$L \leq 4.0$</td><td colspan="3">$N \leq 3$</td></tr><tr><td>$0.07 < W \leq 0.08$</td><td>$L \leq 3.0$</td><td colspan="3">$N \leq 2$</td></tr><tr><td>$0.08 < W$</td><td colspan="3">Define as spot defect</td></tr></table>				Width(mm)	Ignore(mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.05$	Ignore	Ignore			$0.05 < W \leq 0.06$	$L \leq 4.0$	$N \leq 3$			$0.07 < W \leq 0.08$	$L \leq 3.0$	$N \leq 2$			$0.08 < W$	Define as spot defect		
			Width(mm)	Ignore(mm)	Acceptable Qty																												
					A	B	C																										
			$\Phi \leq 0.05$	Ignore	Ignore																												
			$0.05 < W \leq 0.06$	$L \leq 4.0$	$N \leq 3$																												
$0.07 < W \leq 0.08$	$L \leq 3.0$		$N \leq 2$																														
$0.08 < W$	Define as spot defect																																

		CTP Cover Pinhole/ Lack of ink <table><tr><th>Zone Size (mm)</th><th>Acceptable Qty</th></tr><tr><td>$\Phi \leq 0.1$</td><td>C</td></tr><tr><td>$0.1 < \Phi \leq 0.2$</td><td>Ignore</td></tr><tr><td>$0.25 < \Phi \leq 0.3$</td><td>3(distance $\geq 10\text{mm}$)</td></tr><tr><td>$\Phi > 0.35$</td><td>2</td></tr><tr><td></td><td>0</td></tr></table>	Zone Size (mm)	Acceptable Qty	$\Phi \leq 0.1$	C	$0.1 < \Phi \leq 0.2$	Ignore	$0.25 < \Phi \leq 0.3$	3(distance $\geq 10\text{mm}$)	$\Phi > 0.35$	2		0					
Zone Size (mm)	Acceptable Qty																		
$\Phi \leq 0.1$	C																		
$0.1 < \Phi \leq 0.2$	Ignore																		
$0.25 < \Phi \leq 0.3$	3(distance $\geq 10\text{mm}$)																		
$\Phi > 0.35$	2																		
	0																		
	CTP Bonding bubble/ accidented spot <table><tr><th>Size $\Phi(\text{mm})$</th><th colspan="2">Acceptable Qty</th></tr><tr><td></td><td>A</td><td>B</td></tr><tr><td>$\Phi \leq 0.1$</td><td colspan="2">Ignore</td></tr><tr><td>$0.15 < \Phi \leq 0.2$</td><td colspan="2">3(distance $\geq 10\text{mm}$)</td></tr><tr><td>$0.2 < \Phi \leq 0.25$</td><td colspan="2">2</td></tr><tr><td>$\Phi > 0.25$</td><td colspan="2">0</td></tr></table>	Size $\Phi(\text{mm})$	Acceptable Qty			A	B	$\Phi \leq 0.1$	Ignore		$0.15 < \Phi \leq 0.2$	3(distance $\geq 10\text{mm}$)		$0.2 < \Phi \leq 0.25$	2		$\Phi > 0.25$	0	
Size $\Phi(\text{mm})$	Acceptable Qty																		
	A	B																	
$\Phi \leq 0.1$	Ignore																		
$0.15 < \Phi \leq 0.2$	3(distance $\geq 10\text{mm}$)																		
$0.2 < \Phi \leq 0.25$	2																		
$\Phi > 0.25$	0																		
	Assembly deflection	beyond the edge of backlight $\leq 0.2\text{mm}$																	
TP cover broken X : length Y : width Z : height	<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>$X \leq 0.5\text{mm}$</td><td>$Y \leq 0.5\text{mm}$</td><td>$Z < \text{cover thickness}$</td></tr></table> * Circuitry broken is not allowed.	X	Y	Z	$X \leq 0.5\text{mm}$	$Y \leq 0.5\text{mm}$	$Z < \text{cover thickness}$												
X	Y	Z																	
$X \leq 0.5\text{mm}$	$Y \leq 0.5\text{mm}$	$Z < \text{cover thickness}$																	
TP cover broken X : length Y : width Z : height	<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>$X \leq 0.3\text{mm}$</td><td>$Y \leq 0.3\text{mm}$</td><td>$Z < \text{LCD thickness}$</td></tr></table> * Circuitry broken is not allowed.	X	Y	Z	$X \leq 0.3\text{mm}$	$Y \leq 0.3\text{mm}$	$Z < \text{LCD thickness}$												
X	Y	Z																	
$X \leq 0.3\text{mm}$	$Y \leq 0.3\text{mm}$	$Z < \text{LCD thickness}$																	

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

10. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70°C,96h	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1. Air bubble in the LCD; 2. Non-display; 3. Missing segments/line; 4. Glass crack; 5. Current IDD is twice higher than initial value.
Low Temperature Operating	-20°C, 96h	
High Temperature Storage	80°C, 96h	
Low Temperature Storage	-30°C, 96h	
High Temperature & High Humidity Storage	+60°C, 90% RH ,96h	
Thermal Shock (Non-Operation)	-30°C,30 min ↔ 80°C,30 min, Change time: 5min 20CYC.	
ESD Test	C=150pF, R=330,5points/panel Air:±8kV, 5times; Contact:±6kV, 5 times; (Environment: 15°C~35°C, 30%~60%).	
Vibration (Non-Operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM BOX)	

- Remark:
1. The test samples should be applied to only one test item.
 2. Sample size for each test item is 5~10pcs.
 3. For Damp Proof Test, Pure water (Resistance > 10MΩ) should be used.
 4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
 5. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

11. Cautions and Handling Precautions

11.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

11.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0°C to 35°C and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed.
Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.