Display Elektronik GmbH

DATA SHEET

STANDARD OLED/PLED

DEP 128128C3 – RGB (A-TOUCH)

Product Specification ***Version : 03***

11.04.2014

History of Version

Version	Contents	Date	Note
01	NEW VERSION	2012/08/15	SPEC.
02	UPDATE Quality Assurance、Reliability ADD Precautions for Handling、Precautions for Electrical、Precautions for Storage	2013/02/01	
03	Modify Drawing and Reliability	2014/04/11	

C O N T E N T S

2. General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	128xRGBx128	dots
Module dimension (L*W*H)	33.5*71.5*2.1	mm
Active area	26.279*26.284	mm
Dot size	0.0435(W)x0.1855(H)	mm
Dot pitch	0.0685(W)x0.2055 (H)	mm

(2) Controller IC: SSD1351 Controller

(3) Temperature Range

Operating	-40 ~ +70℃
Storage	-40 ~ +85℃

3. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-40	—	+70	℃
Storage Temperature	TST	-40	—	+85	℃
Input Voltage	VI	0.3	—	4.0	V
Operating lifetime			11000(1)		Hrs
Operating lifetime			14000(2)		Hrs

* Note:

(A) Under Vcc = 16.5V, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 90 cd/m:	(2) Setting of 70 cd/m2:
Master contrast setting : 0x0B	Master contrast setting : 0x09
Red contrast setting : 0x70	Red contrast setting : 0x66
Green contrast setting : 0x71	Green contrast setting : 0x6A
Blue contrast setting : 0x94	Blue contrast setting : 0x89
Frame rate : 105Hz	Frame rate : 105Hz
Duty setting : 1/128	Duty setting : 1/128

4. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	—	2.4	3.3	3.5	V
Supply Voltage For Analog	Vcc-V_{SS}	—	16	16.5	17	V
Input High Vol	V_{IH}	—	0.8V_{DD}	—	V_{DD}	V
Input Low Vol	V_{IL}	—	0	—	0.2V_{DD}	V
Output High Vol	V_{OH}	—	0.9V_{DD}	—	V_{DD}	V
Output Low Vol.	V_{OL}	—	0	—	0.1V_{DD}	V
Supply Current For Logic (with built-in positive voltage)	I_{DD}	Normal mode(1)	—	—	220	mA
		Standby mode(2)	—	—	90	
		Sleep mode(3)	—	—	20	

(1) Normal mode condition :All pixel on

- VDD Voltage : 3.3V
- Driving Voltage : 16.5V
- Master contrast setting : 0x0B
- Red contrast setting : 0x70
- Green contrast setting : 0x71
- Blue contrast setting : 0x94
- Frame rate : 105Hz
- Duty setting : 1/128

(2) Normal mode condition : All pixel on ,10% Luminance

- VDD Voltage : 3.3V
- Driving Voltage : 16.5V
- Master contrast setting : 0x04
- Red contrast setting : 0x4E
- Green contrast setting : 0x53
- Blue contrast setting : 0X6E
- Frame rate : 105Hz
- Duty setting : 1/128

(3) Display off.

5. Optical Characteristics

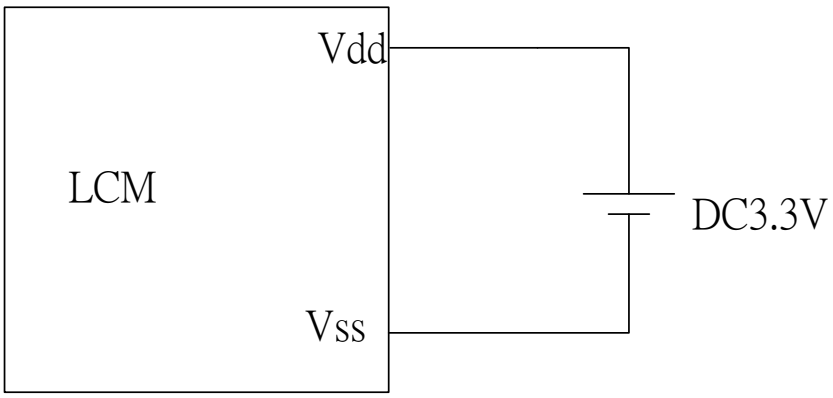
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
View Angle	(V) θ	CR≧20	80	—	80	deg
	(H) φ	CR≧20	80	—	80	deg
Contrast Ratio	CR	—	2000	—	—	—
Response Time	Tr+Tf	—	—	10	—	μs

6. Interface Pin Function

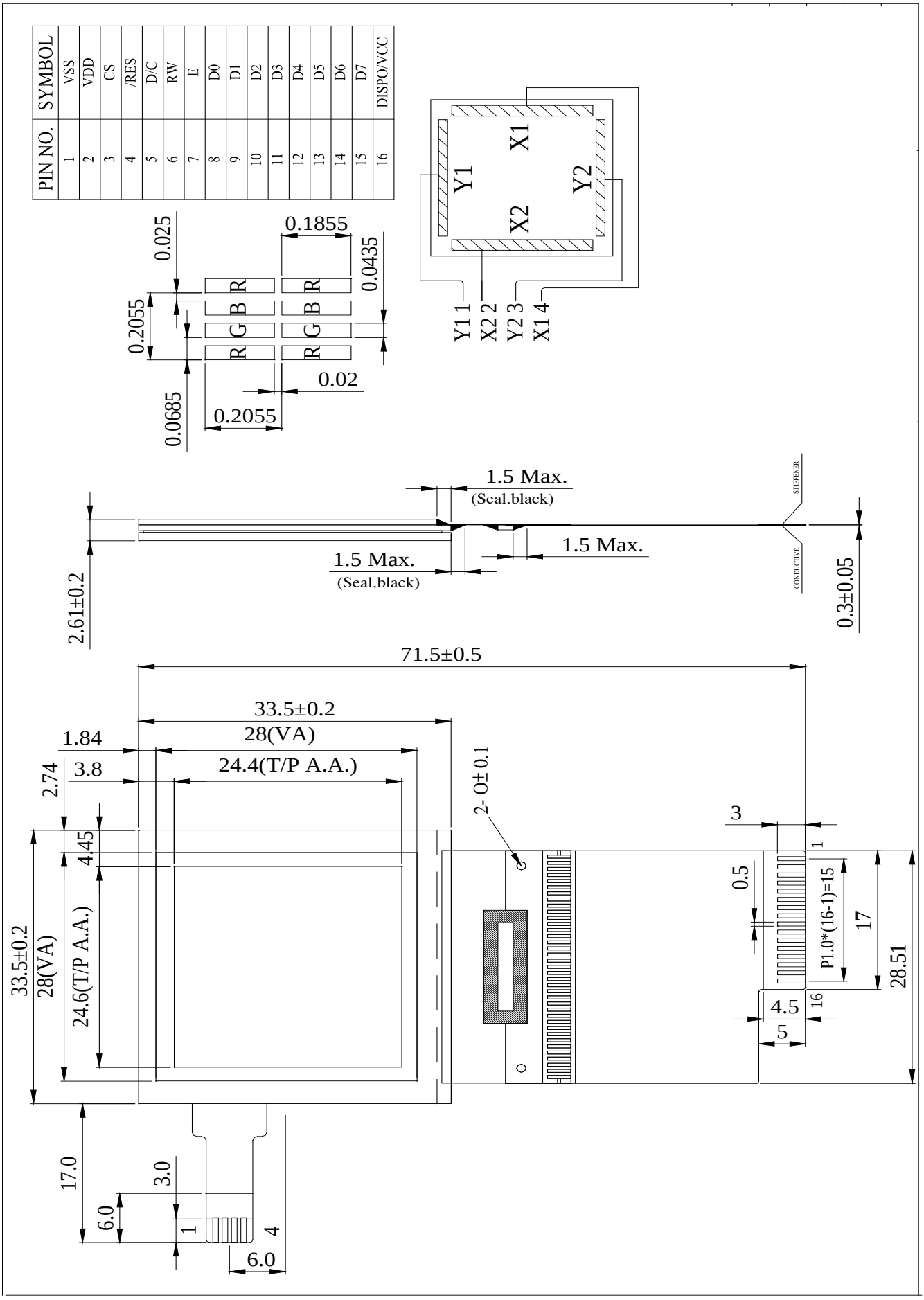
Pin No.	Symbol	Level	Description
1	Vss	0V	Ground
2	Vdd	3.3V	Supply voltage for logic
3	CS	H/L	Chip select pin
4	/RES	H/L	Hardware Reset pin
5	D/C	H/L	H: Data; L: Command.
6	RW	H/L	8080: data write enable pin 6800: Read/Write select pin
7	E	H/L	8080: data read enable pin 6800: Read/Write enable pin
8	DB0	H/L	Data bus line
9	DB1	H/L	Data bus line
10	DB2	H/L	Data bus line
11	DB3	H/L	Data bus line
12	DB4	H/L	Data bus line
13	DB5	H/L	Data bus line
14	DB6	H/L	Data bus line
15	DB7	H/L	Data bus line
16	DISF VCC	H/L H	DISF: VCC Voltage ON/OFF VCC: Supply Voltage For OLED

7. Power supply for LCD Module

LCM operating on "DC 3.3V " input with built-in positive voltage



8. Drawing

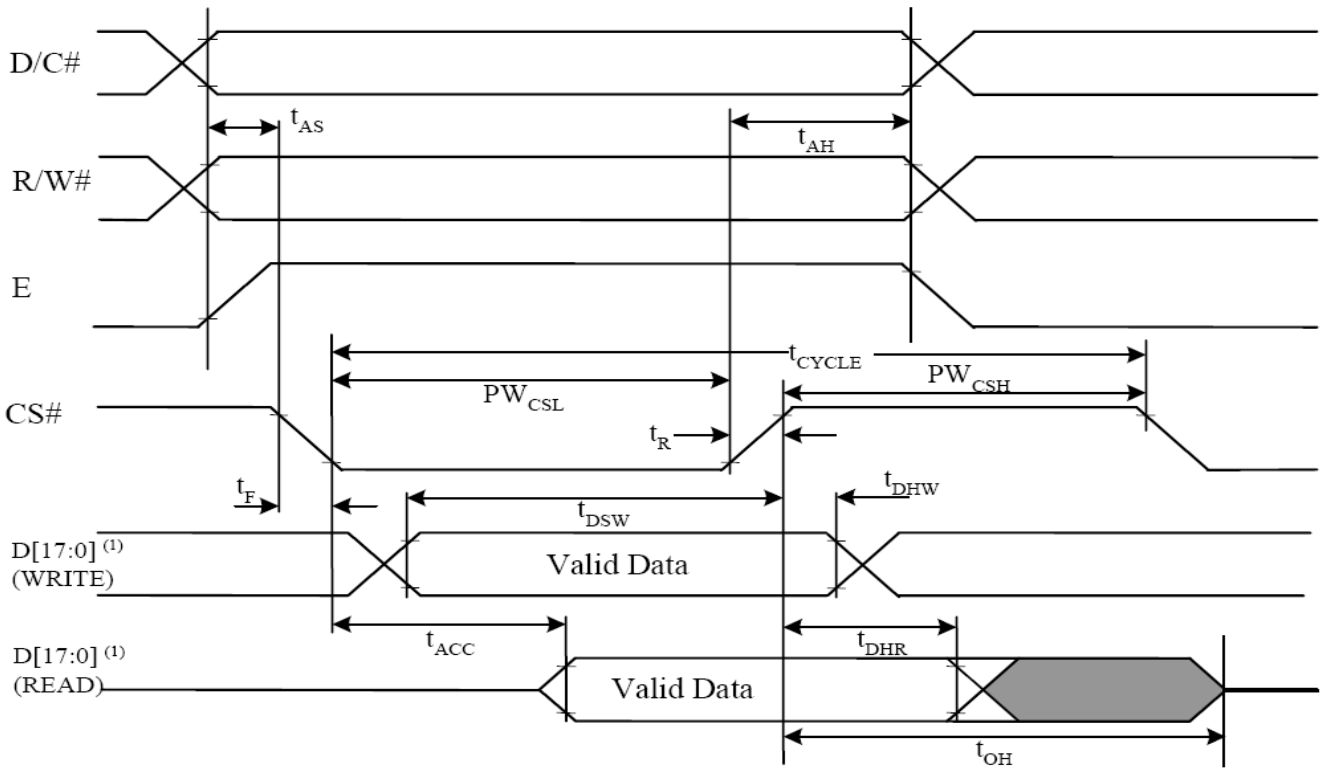

PIN NO. SYMBOL
1 VSS
2 VDD
3 CS
4 /RES
5 D/C
6 RW
7 E
8 D0
9 D1
10 D2
11 D3
12 D4
13 D5
14 D6
15 D7
16 DISPO/VCC
0.025
0.1855
0.0435
0.2055
0.02
0.0685
0.2055
R G B
Y1 X1 Y2 X2
Y1 1 X2 2 Y2 3 X1 4
1.5 Max.
(Seal.black)
STIFFENER
CONDUCTIVE
2.61±0.2
0.3±0.05
71.5±0.5
33.5±0.2
28(VA)
24.4(T/P A.A.)
1.84
2.74
3.8
4.45
2- O± 0.1
24.6(T/P A.A.)
3
0.5
P1.0*(16-1)=15
17
28.51
4.5
5
16
1
17.0
3.0
6.0
4
6.0

9. SSD1351 controller data

9.1 Timing Characteristics

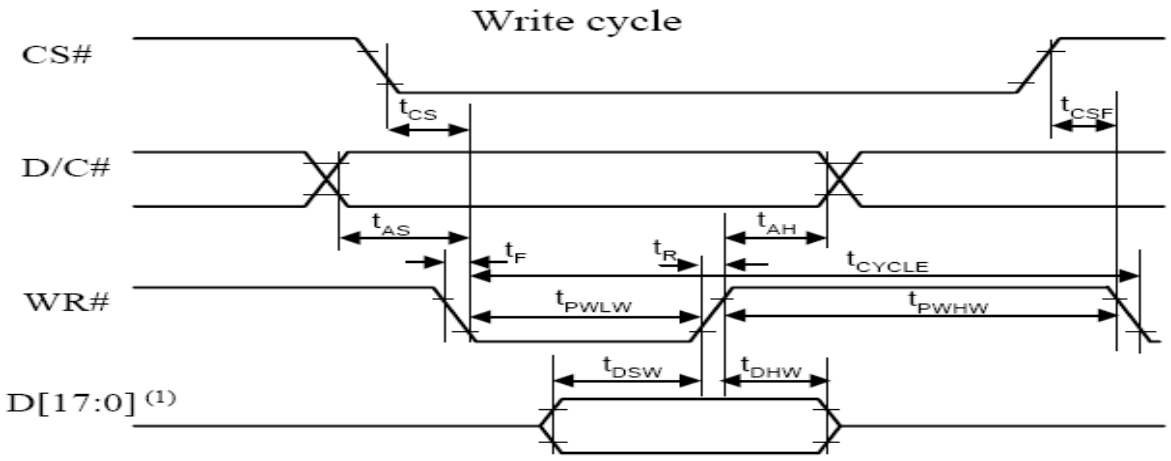
6800 MPU Interface

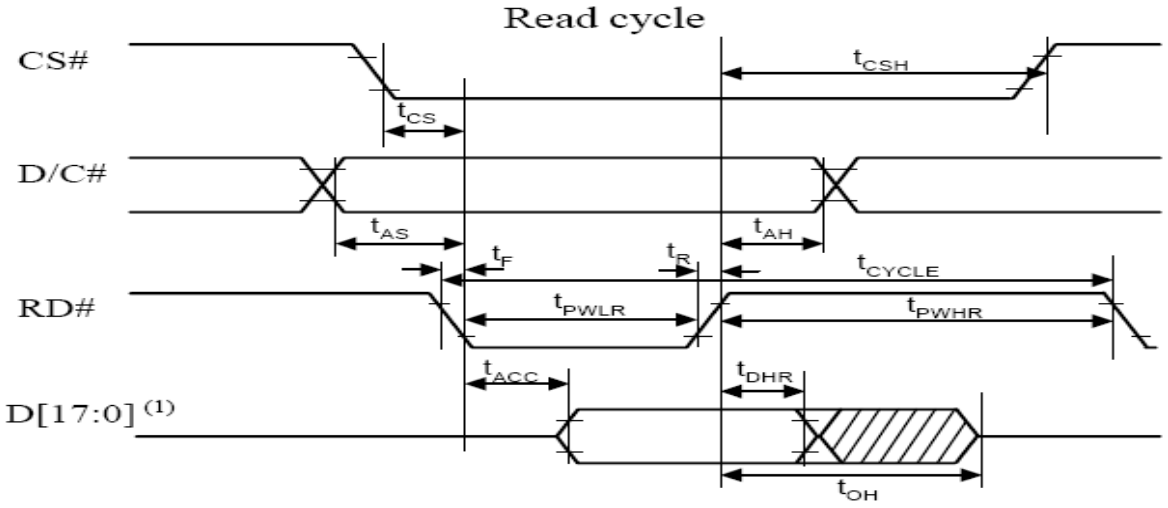
Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



8080 MPU Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns





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9.2 Display Control Instruction

Refer to SSD1351 IC Spec.

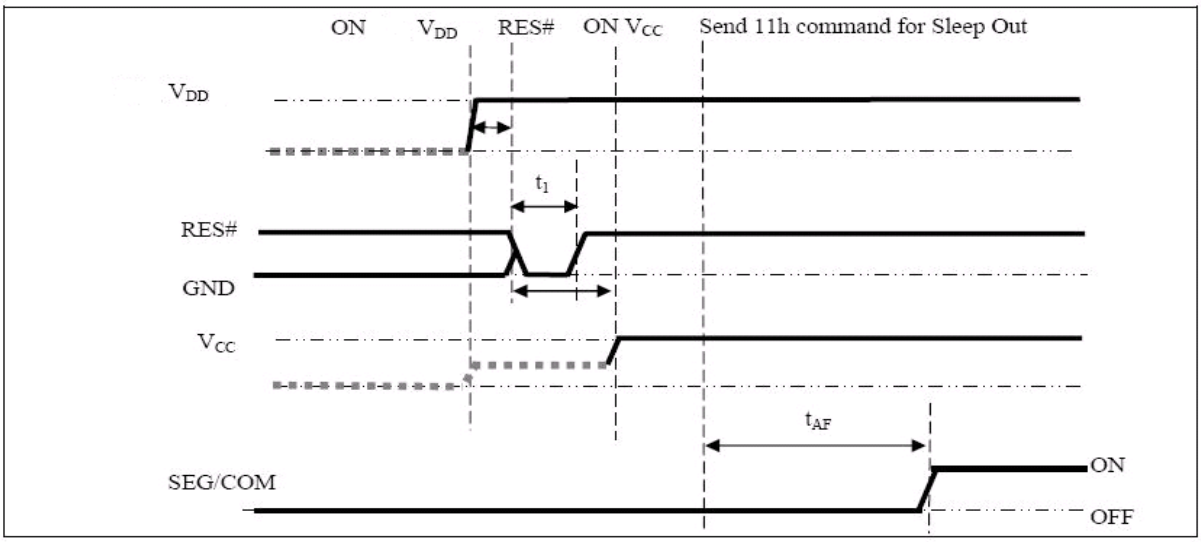
9.3Power ON and OFF sequence

9.3.1POWER ON / OFF SEQUENCE

The following figures illustrate the recommended power ON and power OFF sequence of SSD1351 (assume VCI and VDDIO are at the same voltage level and internal VDD is used).

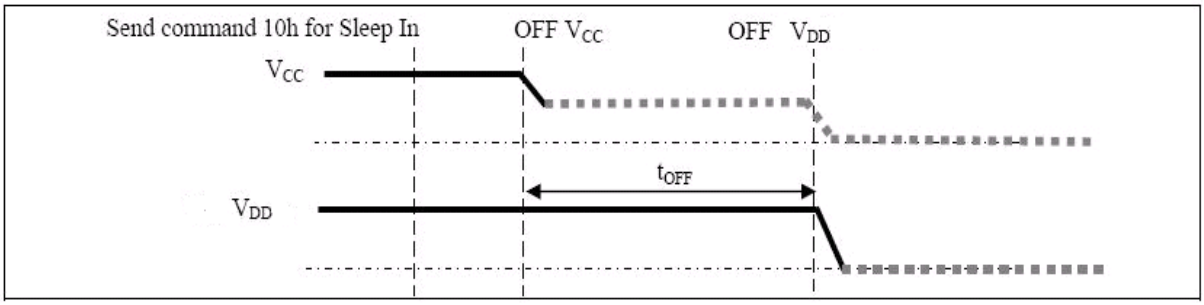
Power ON Sequence

1. Power ON VDD
2. After VDD become stable, set wait time at least 1ms (t0) for internal VDD become stable. Then set RES# pin LOW (logic low) for at least 2us (t1)(4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 2us (t2). Then Power ON VCC. (1)
4. After VCC become stable, send command 11h for Sleep Out. SEG/COM will be ON after 200ms (tAF).



Power OFF Sequence

1. Send command AEh for display OFF.
2. Power OFF VCC. (1), (2)
3. Wait for tOFF. Power OFF VDD (where Minimum tOFF=80ms (3),Typical tOFF=100ms)



Note:

(1) Since an ESD protection circuit is connected between VCI,VDDIO and VCC,VCC becomes lower than VCI whenever VCI,VDDIO is ON and VCC is OFF as shown in the dotted line of VCC in above figures.
(2) VCC should be disabled when it is OFF.
(3) VCI, VDDIO should not be Power OFF before VCC Power OFF.
(4) The register values are reset after t1.
(5) Power pins(VDDIO, VCC) can never be pulled to ground under any circumstance.

9.3.2 COMMAND TABLE

Refer to IC Spec.: SSD1351

9.3.3 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 128x128x18bits. For mechanical flexibility , re-mapping on both Segment and Common outputs can be selected by software . Each pixel has 18-bitdata. Each sub-pixels for color A, B and C have 6bits.The arrangement of data pixel in graphic display data RAM is shown below.

262k Color Depth Graphic Display Data RAM Structure

Segment	Normal	0			1			2	.....	.....	126	127			
Address	Remapped	127			126			125	.....	.....	1	0			
Color		A	B	C	A	B	C	A			C	A	B	C	
Data Format / Common Address		A5	B5	C5	A5	B5	C5	A5	.....	.....	C5	A5	B5	C5	
		A4	B4	C4	A4	B4	C4	A4	.....	.....	C4	A4	B4	C4	
		A3	B3	C3	A3	B3	C3	A3	.....	.....	C3	A3	B3	C3	
		A2	B2	C2	A2	B2	C2	A2	.....	.....	C2	A2	B2	C2	
		A1	B1	C1	A1	B1	C1	A1	.....	.....	C1	A1	B1	C1	
		A0	B0	C0	A0	B0	C0	A0	.....	.....	C0	A0	B0	C0	Common output
Normal	Remapped														
0	127	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM0
1	126	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM1
2	125	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM2
3	124	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM3
4	123	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM4
5	122	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM5
6	121	6	6	no of bits in this cell			6	6	.....	.....	6	6	6	6	COM6
7	120								.....	.....	6	6	6	6	COM7
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	:
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	:
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	:
123	4	6	6	6	6	6	6	6	.....	.....	6	6	6	6	:
124	3	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM124
125	2	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM125
126	1	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM126
127	0	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM127

SEG output	SA0	SB0	SC0	SA1	SB1	SC1	SA2	.....	.....	SC126	SA127	SB127	SC127

10 Quality Assurance

10.1 Inspection conditions

1. The inspection and meaurement are performed under the following conditions,
2. unless otherwise specified.
3. Temperature: 25±5°C
4. Humidity: 50±10%R.H.
5. Distance between the panel and eyes of the inspector≧30cm

10.2 Inspection Parameters

Severity	Inspection Item	Defect	Remark
Major Defect	1. Panel	(1) Non-displaying	
		(2) Line defects	
		(3) Malfunction	
		(4) Glass cracked	
	2. Film	(1) Film dimension out of specification	Can not be assembled
	3. Dimension	(1) Outline dimension out of specification	
Minor Defect	1. Panel	(1) Glass scratch	Appearance defect
		(2) Glass cutting NG	
		(3) Glass chip	
	2. Polarizer	(1) Polarizer scratch	
		(2) Stains on surface	
		(3) Polarizer bubbles	
	3. Displaying	(1) Dim spot、Bright spot、dust	
	4. Film	(1) Damage (2) Foreign material	

<table>
<tr><th>Description</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>1. Glass scratch</td><td>
<table>
<tr><th>Width (mm)
W</th><th>Length (mm)
L</th><th>number of pieces permitted</th></tr>
<tr><td>W≦0.03</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td>0.03＜ W≦0.05</td><td>L≦3</td><td>3</td></tr>
<tr><td>0.05＜ W</td><td>------</td><td>None</td></tr>
<tr><td>beyond A.A.</td><td>------</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2. Polarizer bubble</td><td>
<table>
<tr><th>Size</th><th>number of pieces permitted</th></tr>
<tr><td>Φ ≦0.2</td><td>Ignore</td></tr>
<tr><td>0.2＜Φ ≦0.5</td><td>2</td></tr>
<tr><td>0.5＜Φ</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>3. Dimming spot、Lighting spot、Dust</td><td>
<table>
<tr><th>average</th><th>number of</th></tr>
<tr><td>D ≦0.1</td><td>Ignore</td></tr>
<tr><td>0.1＜ D ≦0.15</td><td>2</td></tr>
<tr><td>0.15＜ D ≦0.2</td><td>1</td></tr>
<tr><td>0.2 ＜ D</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
D=(long diameter + short diameter)/2.
Pixel off is not allowed.
</td><td>Minor</td></tr>
</table>

10.3 WARRANTY POLICY

Our company will provide one-year warranty for the products only if under specification operating conditions.
If there are functional defects found during the period of warranty, the defective products would be replaced on a one-to-one basis.
Our company would not be responsible for any direct/indirect liabilities consequential to any parties.

10.4 MTBF

10.4.1 .MTBF based on specific test condition is 11K hours.

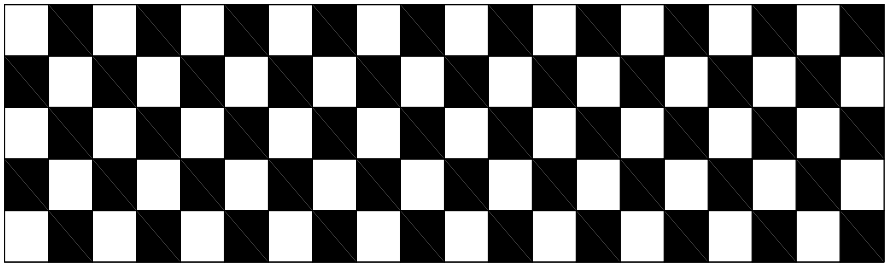
10.4.2 Test Condition:

10.4.2.1 Supply Voltage: Vcc=16.5V

10.4.2.2 Luminance: 90cd/m2

10.4.2.3 Operation temperature and humidity:25 ℃ and 50%RH

10.4.2.4 Run-Patterns:



10.4.3 Test Criteria:

Luminace has decayed to less than 50% of the initial measured luminance.

11.Reliability

■Content of Reliability Test

NO.	Items.	Specification	Applicable Standard
1	High temp. (Non-operation)	85°C, 240hrs	——
2	High temp. (Operation)	70°C, 120hrs	——
3	Low temp. (Operation)	-40°C, 120hrs	——
4	High temp. / High. humidity (Operation)	65°C, 90%RH, 96hrs	——
5	Thermal shock(Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 20 cycles.	——
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	——

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1 & 4 & 5.

Criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: >50% of initial value.
4. Current consumption : within ±50% of initial value.

Reliability Test

Our company only guarantees the reliability of the panel under the test conditions and durations listed in the specification, and is not responsible for any test results that are conducted using more stringent conditions and/or with lengthened durations. Also, when the testing the panel in a chamber or oven, make sure they won't produce any condensation on the panel, especially on the electrical leads, before lighting on the panel to see if it passes the test. Also the panel should rest for about an hour at room temperature and pressure before the measurement, as indicated in the specification. Be aware that one should use fresh panel for each of the reliability test items listed in the specification, in other words, don't use the panels that were tested for subsequent tests.

12.Precautions for Handling

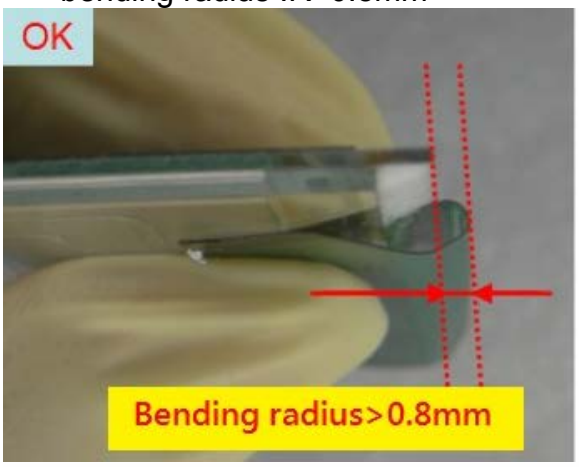
12.1 When handling the module, wear powder-free antistatic rubber finger cots, and be careful not to bend and twist it.

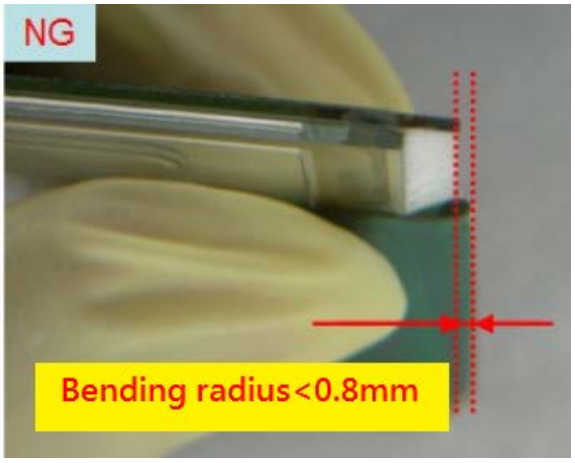
12.2 The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, or being dropped from a height.

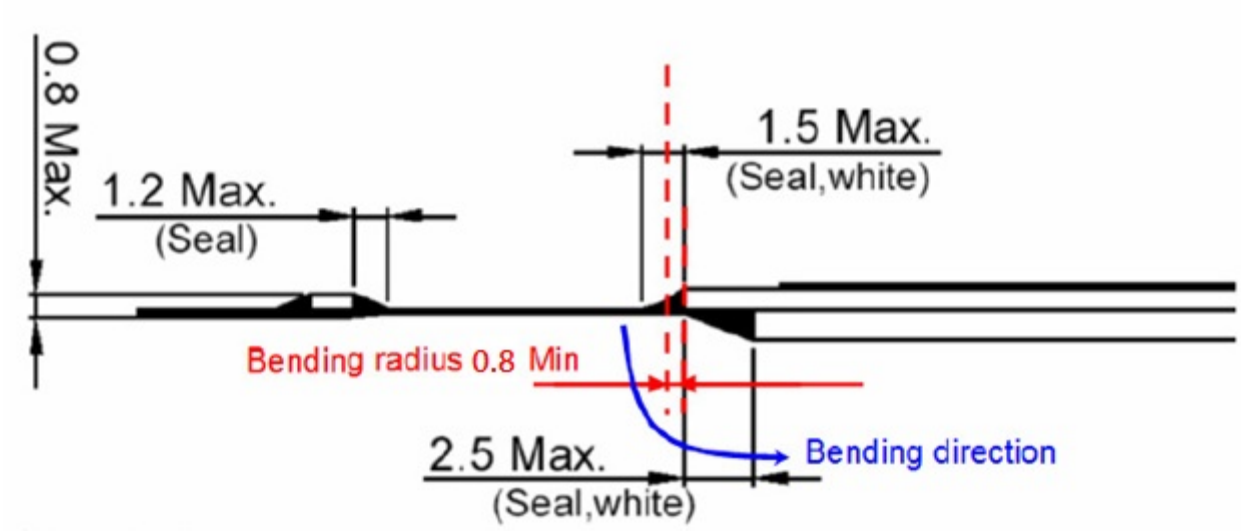
12.3 The OLED module is an electronic component and is subject to damage caused by Electro Static

Discharge (ESD) and hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Also, ground the tools being used for panel assembly and make sure the working environment is not too dry to cause ESD problems. (See the photos below).

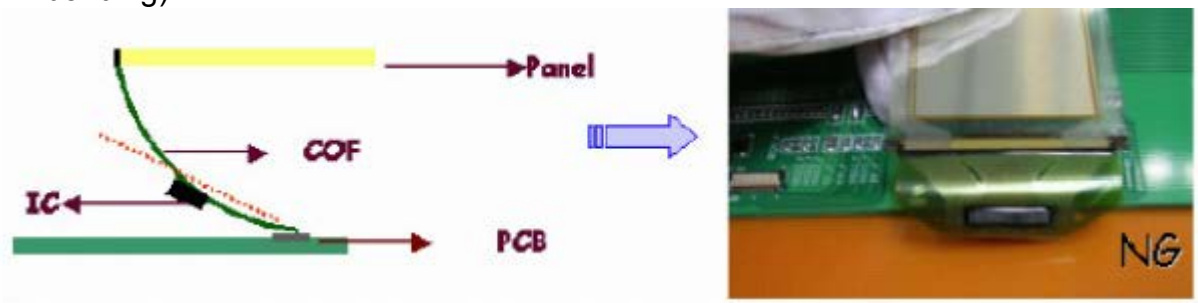
12.4 Please do not bend the film near the substrate glass.(this could cause film peeling and COF damage) and the peeling strength about 600g/cm, the bending <20times and the bending radius :R>0.8mm



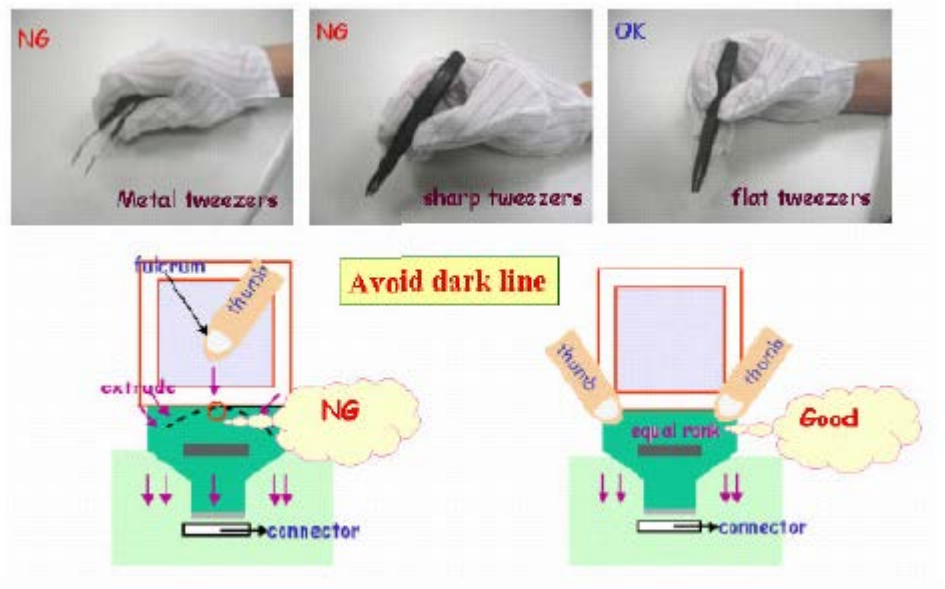




12.5 Avoid bending the film at IC bonding area.(>1.5mm)(this could damage the ILB bonding)



12.6 Use both thumbs to insert COF into the connector when assembling the panel. See the photo on the far right below for correct insertion of the film into the connector (one-handed insertion exerts uneven force on the film and could cause its breakage, photo on the left)



12.7 Do not wipe the pin of film with the dry or hard materials that will damage the surface. When cleaning the display surface, use soft cloth solvent and wipe gently (Recommend solvent: IPA, alcohol), and do not wipe the display with dry or hard materials that will damage the polarizer surface and do not use the solvent like: Water, Acetone, Aromatic

13. Precautions for Electrical

13.1.Design using the settings in the specification

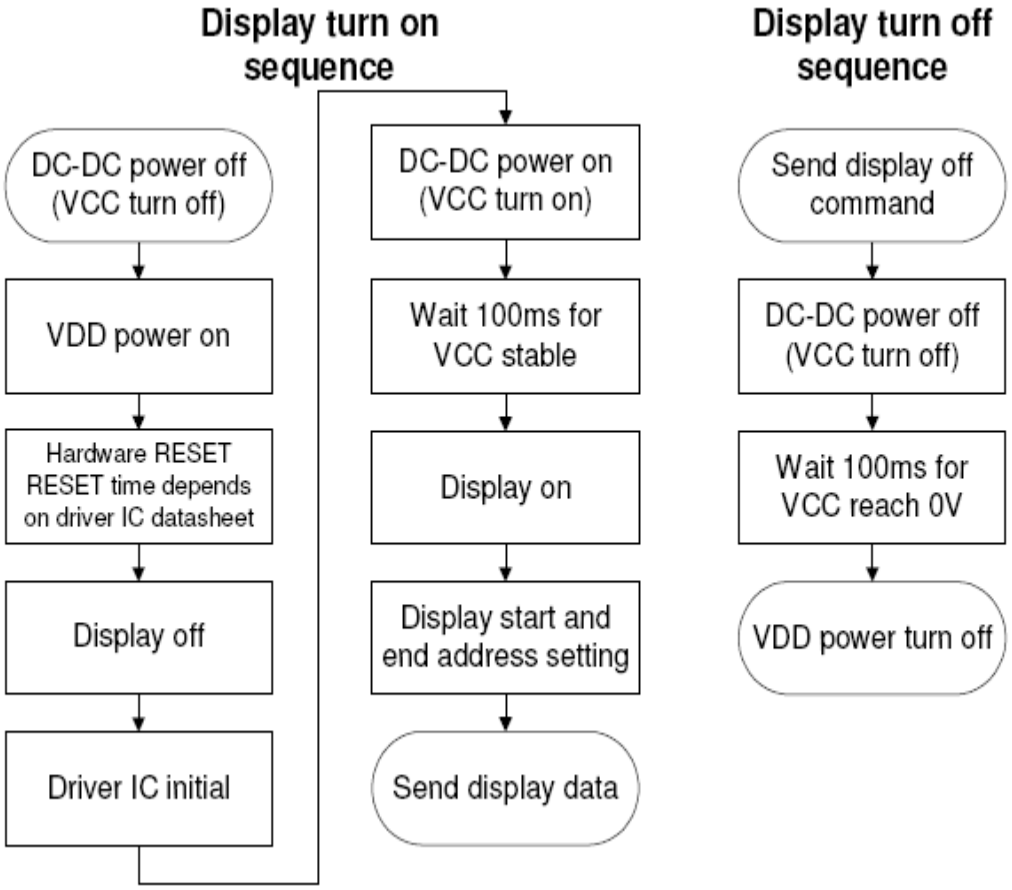
It is extremely important to design and operate the panel using the settings listed in the specification. This includes voltage, current, frame rate, duty cycle... etc. Operation of the OLED outside the specified range in the specification should be entirely avoided to ensure proper operation of the OLED.

13.2.Maximum Ratings

To ensure proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.

13.3 Power on/off procedure

Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, could cause OLED panel malfunctioning.



13.4 Power savings

To save power consumption of the OLED, one can use partial display or sleep mode when the panel is not fully activated. Also, if possible, make maximum use of black background to save power. The OLED is a self-luminous device, and a particular pixel cluster or image can be lit on via software control, so power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright

Mode, Normal Operation Mode, and Sleeping Mode.
The power consumption is almost in direct proportion to the brightness of the panel, and also in direct proportion to the number of pixels lit on the panel, so the customer can save the power by the use of black background and Sleeping Mode. One benefit from using these design schemes is the extension of the OLED lifetime.

13.5 Residual Image (Image Sticking)

The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. The time when image sticking happens depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following three strategies to minimize image sticking

13.5.1 Employ image scrolling or animation to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.

13.5.2 Minimize the use of all-pixels-on or full white background in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays

13.5.3 If in the reliability test when a static logo is used, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns

14. Precautions for Storage

Although the storage conditions and guarantee period are indicated in the specification, it is advisable to store the packed cartons or packages at 23℃±5℃,55%±10%RH, Do not store the OLED module under direct sunlight or UV light and for best panel performance, unpack the cartons and start the production with the panels within **one months** after the reception of them.