Display Elektronik GmbH

DATA SHEET

LCD MODULE

DEP 128064B-Y

Product Specification **Version: 3.1**

26.06.2013

Revised History			
Part Number	REV	Revision Content	Revised
DEP 128064B-Y	0	Original	10.01.2012
DEP 128064B-Y	1	Add Version	10.01.2012
DEP 128064B-Y	2	Add Interface	03.02.2012
DEP 128064B-Y	3	Change OLED-Panel	30.05.2013
DEP 128064B-Y	3.1	Correct CIE Parameter	26.06.2013

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1 Basic Specifications

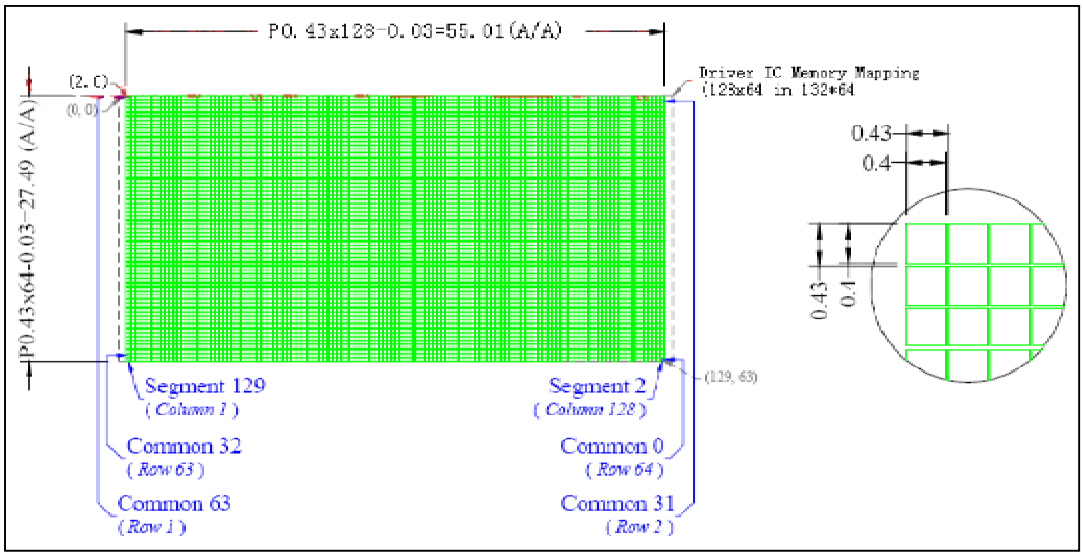
1.1 Display Specifications

Display Mode	: Passive Matrix OLED, Yellow
Resolution	: 128 x 64 Dots
Interface	: 8-Bit-8080 (Standard Configuration)
	: 8-Bit-6800, SPI, I2C (optional)
Driver IC	: SSD1305 (Solomon Systech)

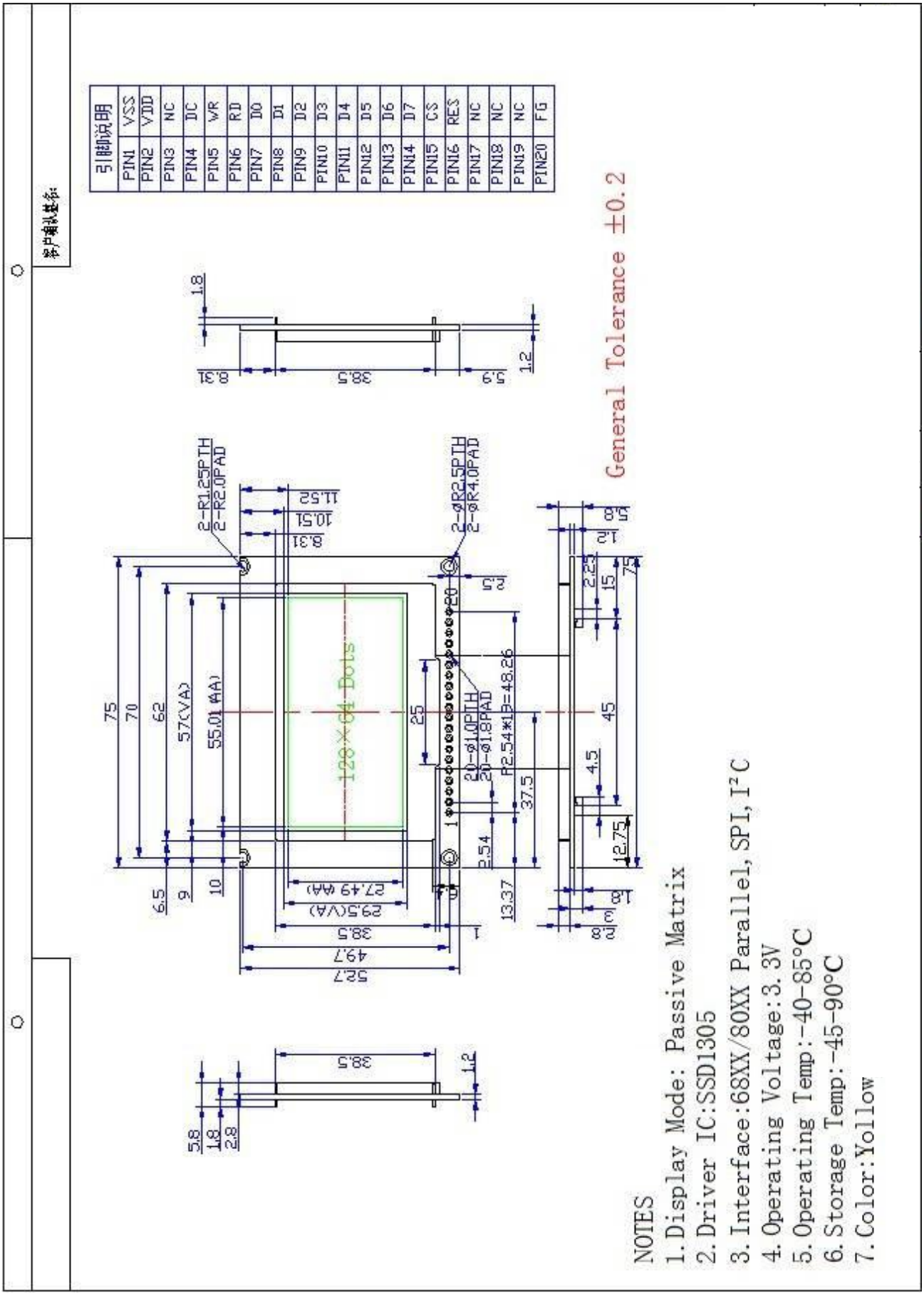
1.2 Mechanical Specifications

Outline Dimension	: 70.50 x 49.60 x 6.50 mm (max.)
Viewing-Area	: 57.01 x 29.49 mm
Active-Area	: 55.01 x 27.49 mm
Resolution	: 128 x 64
Dot-Size	: 0.40 x 0.40 mm
Dot-Gap	: 0.03 mm

1.3 Active Area & Pixel Construction



1.4 Mechanical Drawing



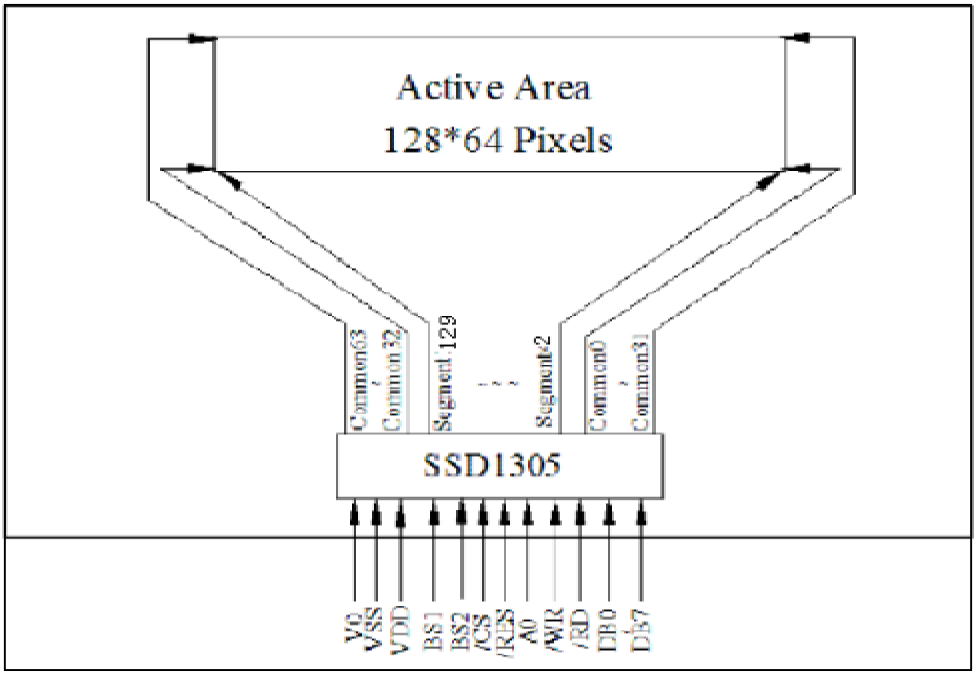
1.5 Pin Definition

PIN-NO	SYMBOL	I/O	FUNCTION
1	Vss	P	Ground of Logic Circuit. This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.
2	Vdd	3.3V~5.0V	Power Supply for Display Module Circuit. This is a voltage supply pin. It connected to external source.
3	NC	-	Not Connected
4	/DC	I	Data / Command Control. This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
5	/WR	I	Read/Write Select or Write This pin is MCU interface input, When interfacing to an 68XX-series microprocessor, this pin will be used as Read/Write (R/W) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode. When 80XX interface mode is selected, this pin will be the Write (WR) input. Data write operation is initiated when this pin is pulled low and the CS is pulled low.
6	/RD	I	Read/Write Enable or Read This pin is MCU interface input, When interfacing to an 68XX-series microprocessor, this pin will be used as the Enable(E) signal. Read/Write operation is initiated when this pin is pulled high and the CS is pulled low. When connecting to an 80XX microprocessor, this pin receives the Read(RD) signal. Data read operation is initiated when this pin is pulled low CS is pulled low.

<table>
<tr><td>7-14</td><td>D0…D7</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.</td></tr>
<tr><td>15</td><td>/CS</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>16</td><td>/RESET</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>17</td><td>NC (BS1)</td><td>H/L</td><td rowspan="2">Communicating Protocol Select
These pins MCU interface selection input. See the following table:
<table><tr><td></td><td>68XX</td><td>80XX</td><td>I2C</td><td>SPI</td></tr><tr><td>BS1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>BS2</td><td>1</td><td>1</td><td>0</td><td>0</td></tr></table></td></tr>
<tr><td>18</td><td>NC (BS2)</td><td>H/L</td></tr>
<tr><td>19</td><td>NC</td><td>-</td><td colspan="3">Float or connect to Vss</td></tr>
<tr><td>20</td><td>FG</td><td>0V</td><td colspan="3">IT connected to external Ground.</td></tr>
</table>

INTERFACE-SELECTION-Note:
Set the pin 17/18 unconnected or use it as signal to setup the BS1/BS2 configuration.
Standard configuration is 8-Bit-Parallel 80XX Interface (BS1=1 and BS2=1)

1.6 Elements Block Diagram



(MCU Interface Selection: By the Module internal of the Pin BS1 and Pin BS2) Pins Connected to MCU interface: D7~D0, /RD, /WR, /CS, A0 and /RES.

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VBAT	3.0	5	V
Driver Supply Voltage	Vcc	0	15	V
Vcc Supply Current	Icc	-	28	mA
Operating Temperature	Top	-40	+85	°C
Storage Temperature	Tstg	-45	+90	°C

Note 1: All the above voltage are on the basis of “GND=0V”.

Note 2: When this module is used beyond the above absolute maximum

Ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

3. Electrical Characteristics

3.1 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VBAT		2.8	3.0	5	V
High Level Input	VIH	Iout =100Ua 3.3MHz	0.8xVdd	-	Vdd	V
Low Level Input	VIL	Iout =100Ua 3.3MHz	0	-	0.2xVdd	V
Supply Current	IVBAT	Note	-	90	--	mA
Display voltage	VCC	Ta = 25°C	12.0	12.5	13	V

Note: V_{DD}=3.0V,V_{CC}=12.5V (V_{DD} and V_{CC} Supply by the module internal generate) 100% Display Area Turn on.

3.2 Optics & Electrical Characteristics

CHARACTERISTICS	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Brightness	Lbr	With Polarizer	100	-	-	cd/m2
C.I.E. (Green)	(X) (Y)	C.I.E. 1931	0.45 0.46	0.49 0.50	0.53 0.54	
Dark Room Contrast	CR		2000:1	-	-	-
Viewing Angle			160°	-	-	Degree

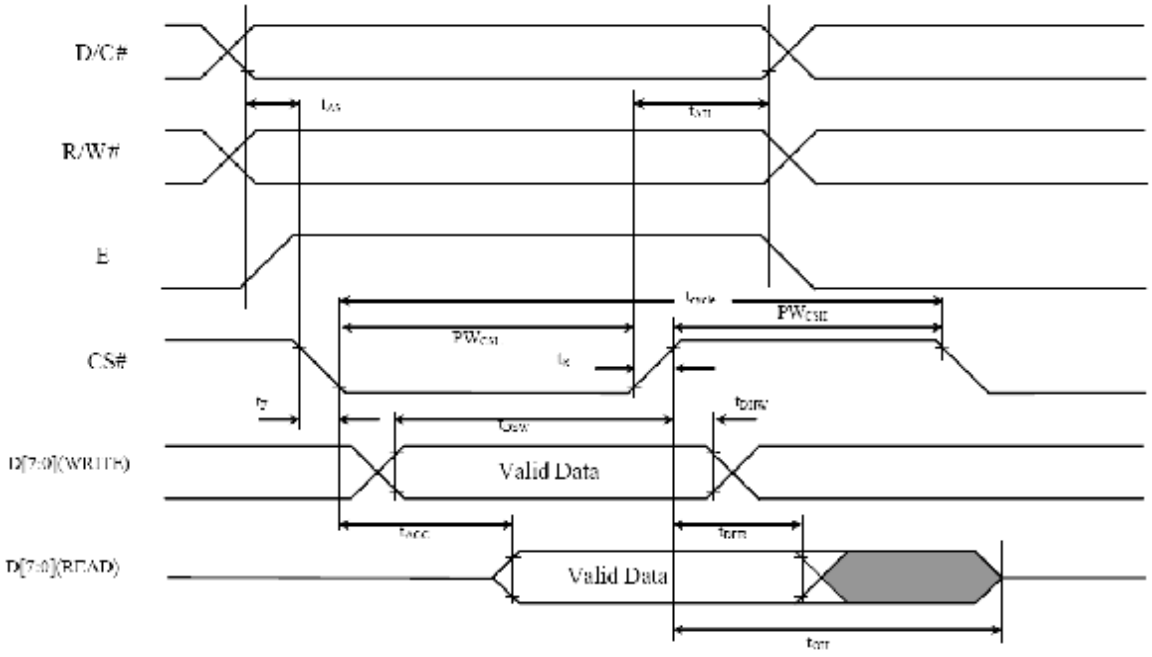
Optical measurements taken at Vdd = 2.8Volt. Vcc=12.5Volt and software configuration following section 4.8 “Software Initial Settings”.

3.3 AC Characteristics

3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
tcycle	Clock Cycle Time(write cycle)	300	-	ns
PWcsl	Control Pulse Low Width(writer cycle)	60	-	ns
PWcsh	Control Pulse High Width(write cycle)	60	-	ns
tcycle	Clock Cycle Time(read cycle)	200	-	ns
PWcsl	Control Pulse Low Width(read cycle)	120	-	ns
PWcsh	Control Pulse High Width(read cycle)	60	-	ns
tAS	Address Setup Time	0	-	ns
tAH	Address Hold Time	0	-	ns
tDSW	Data Setup Time	40	-	ns
tDHW	Data Hold Time	7	-	ns
tACC	Access Time	-	140	ns
tOH	Output Disable Time	-	70	ns
tR	Rise Time	-	40	ns
tF	Fall Time	-	40	ns

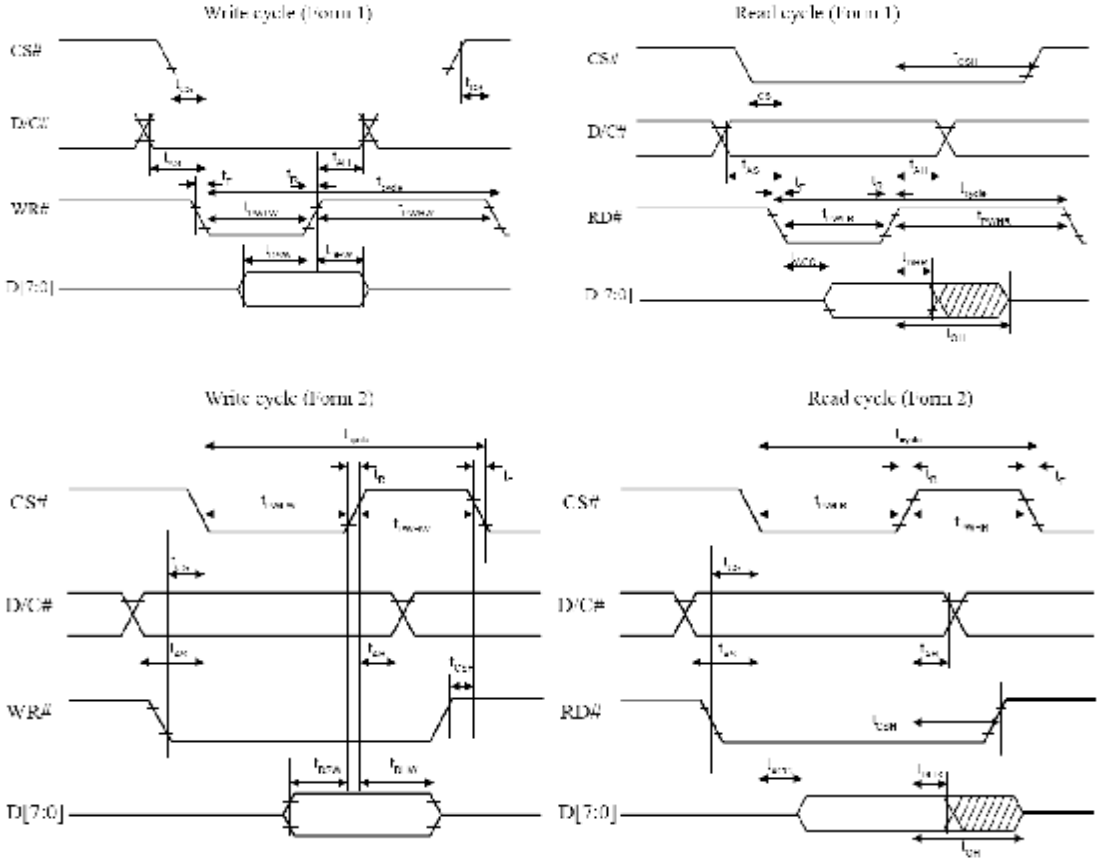
*(V_{DD}-V_{SS}=2.4V to 3.5V, V_{DDIO}= V_{DD}, TA=25°C)



3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
tcycle	Clock Cycle Time	300	-	ns
tAS	Address Setup Time	10	-	ns
tAH	Address Hold Time	0	-	ns
tDSW	Write Data Setup Time	40	-	ns
tDHW	Write Data Hold Time	7	-	ns
tDHR	Read Data Hold Time	20	-	ns
tOH	Output Disable Time	-	70	ns
tACC	Access Time	-	140	ns
PWCSL	Chip Select Low Pulse Width(Read) Chip Select Low Pulse Width(write)	120 60	-	ns
PWCSH	Chip Select High Pulse Width(Read) Chip Select High Pulse Width(write)	60 60	-	ns
tR	Rise Time	-	40	ns
tF	Fall Time	-	40	ns
tcs	Chip select setup time	0	-	ns
tCSH	Chip select hold time to read signal	0	-	ns
tCSF	Chip select hold time	20	-	ns

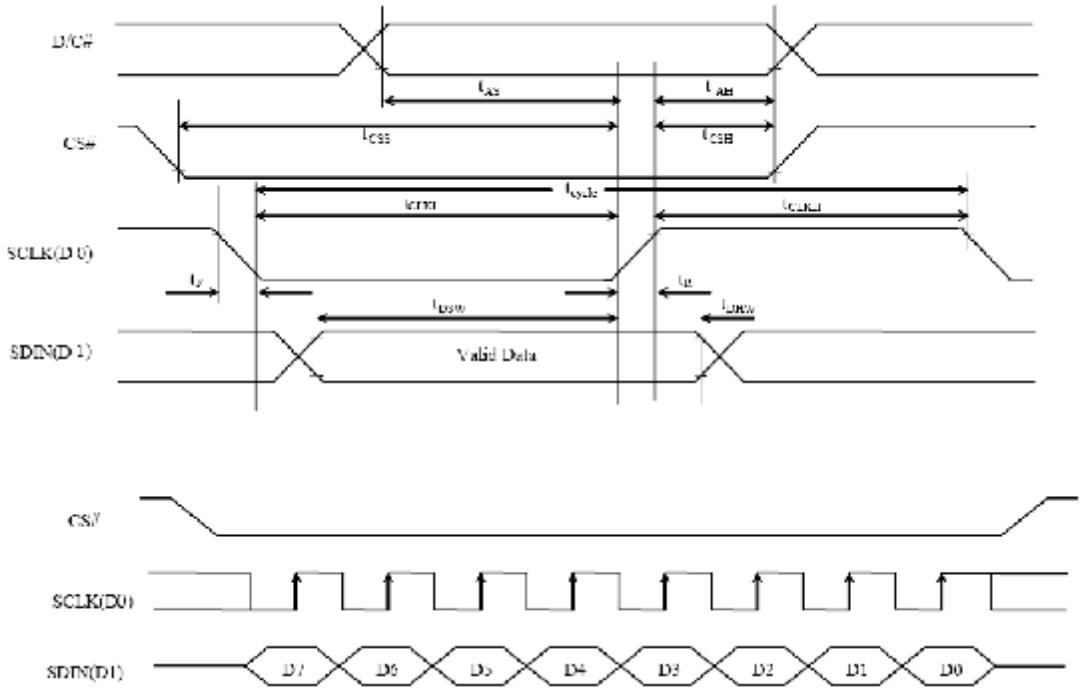
*(V_{DD}-V_{SS}=2.4V to 3.5V,V_{DDIO}= V_{DD}, TA=25°C)



3.3.3 Serial Interface Timing Characteristics (optional):

Symbol	Description	Min	Max	Unit
tcycle	Clock Cycle Time	250	-	ns
tAS	Address Setup Time	150	-	ns
tAH	Address Hold Time	150	-	ns
tCSS	Chip Select Setup Time	120	-	ns
tCSH	Chip Select Hold Time	60	-	ns
tDSW	Write Data Setup Time	50	-	ns
tDHW	Write Data Hold Time	15	-	ns
tCLKL	Clock Low Time	100	-	ns
tCLKH	Clock High Time	100	-	ns
tR	Rise Time	-	40	ns
tF	Fall Time	-	40	ns

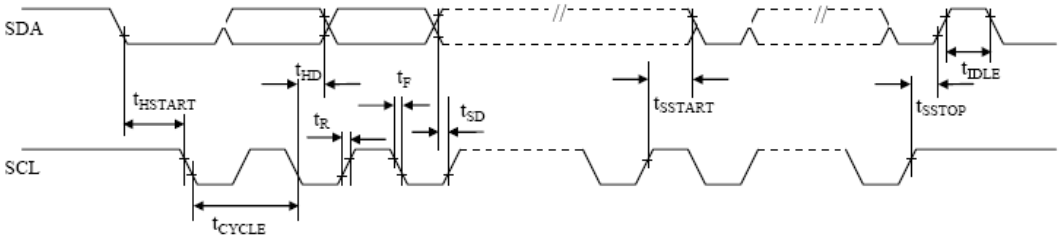
*(V_{DD}-V_{SS}=2.4V to 3.5V, V_{DDIO}= V_{DD}, TA=25°C)



3.3.4 I2C Interface Timing Characteristics (optional):

Symbol	Description	Min	Max	Unit
tcycle	Clock Cycle Time	2.5	-	us
tHSTART	Start condition Hold Time	0.6	-	us
tHD	Data Hold Time(for "SDAOUT"pin) Data Hold Time(for "SDIN"pin)	0 300	-	ns ns
tSD	Data Setup Time	100	-	ns
tSSTART	Start condition Setup Time(Only relecant for a repeated Start condition)	0.6	-	us
TSSTOP	Stop condition Setup Time	0.6	-	us
tR	Rise Time for data and clock pin	-	300	ns
tF	Fall Time for data and clock pin	-	300	ns
tIDLE	Idle Time before a new transmission can start	1.3	-	us

*(V_{DD}-V_{SS}=2.4V to 3.5V,V_{DDIO}= V_{DD}, TA=25°C)



4. Functional Specification

MCU Interface Selection:

MCU Interface assignment under different bus interface mode:

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#
I²C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	Tie LOW			SA0	RES#

4.1 MCU parallel 6800-Series Interface

The parallel interface consists of 8 bi-directional data pins (DB[7:0]), R/W, D/C, E and /CS.A LOW in R/W indicates WRITE operation and HIGH in R/W indicates READ operation. A LOW in D/C indicates COMMAND read/write and HIGH in D/C indicates DATA read/write. The E input serves as data latch signal while /CS is LOW. Data is latched at the falling edge of E signal.

Control pins of 6800 interface

Function	E	R/W	/CS	D/C
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

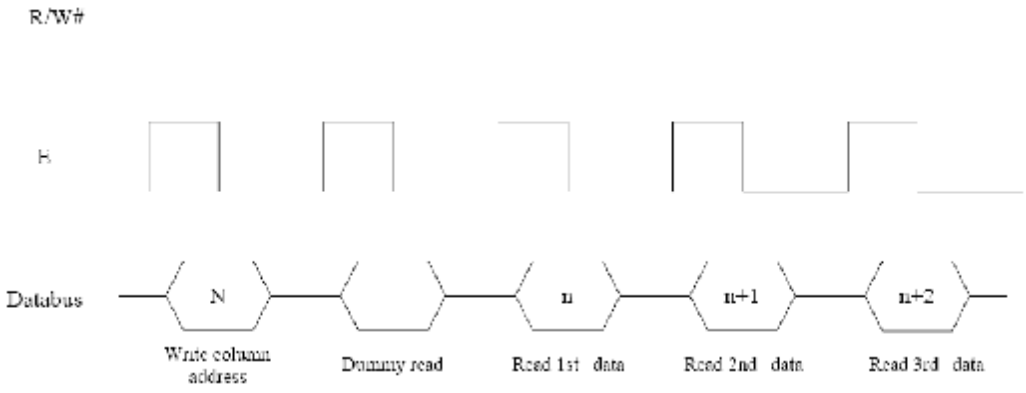
Note (1) ↓ stands for falling edge of signal

H stands for HIGH in signal

L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown as follows.

Data read back procedure - insertion of dummy read



4.2 MCU parallel 8080-Series Interface

The parallel interface consists of 8 bi-directional data pins (DB[7:0]), /RD, /WR, D/C and /CS.A LOW in A0 indicates COMMAND read/write and HIGH in D/C indicates DATA read/write. A rising edge of /RD input serves as a data READ latch signal while /CS is kept LOW.A rising edge of /WR input serves as a data/command WRITE latch signal while /CS is kept LOW.

Control pins of 8080 interface (Form 1)

Function	/RD	/WR	/CS	D/C
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note (1) ↑ stands for rising edge of signal

(2) H stands for HIGH in signal

(3) L stands for LOW in signal

(4) Refer to Figure 13-2 for Form 1 8080-Series MPU Parallel Interface Timing Characteristics

Alternatively, /RD and /WR can be keep stable while /CS serves as the data/command latch signal.

Control pins of 8080 interface (Form 2)

Function	/RD	/WR	/CS	D/C
Write command	H	L	↑	L
Read status	L	H	↑	L
Write data	H	L	↑	H
Read data	L	H	↑	H

Note

(1) ↑ stands for rising edge of signal

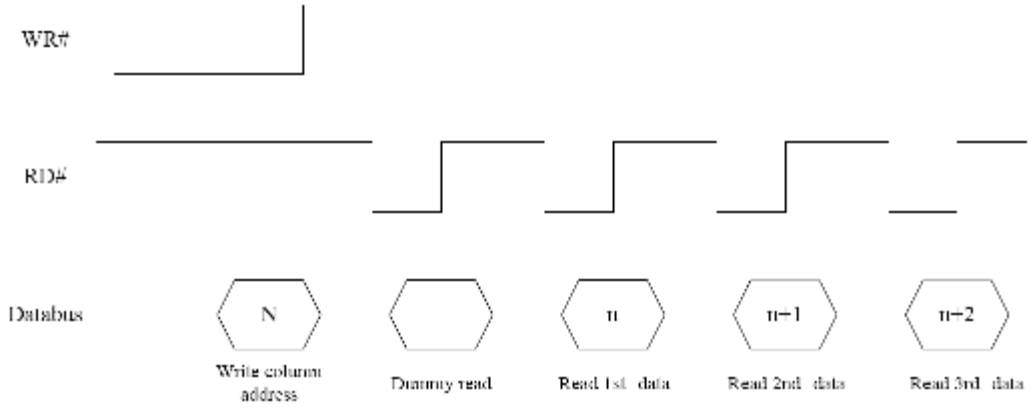
(2) H stands for HIGH in signal

(3) L stands for LOW in signal

(4) Refer to Figure 13-3 for Form 2 8080-Series MPU Parallel Interface Timing Characteristics

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown as follows.

Display data read back procedure - insertion of dummy read



4.3 MCU Serial Interface

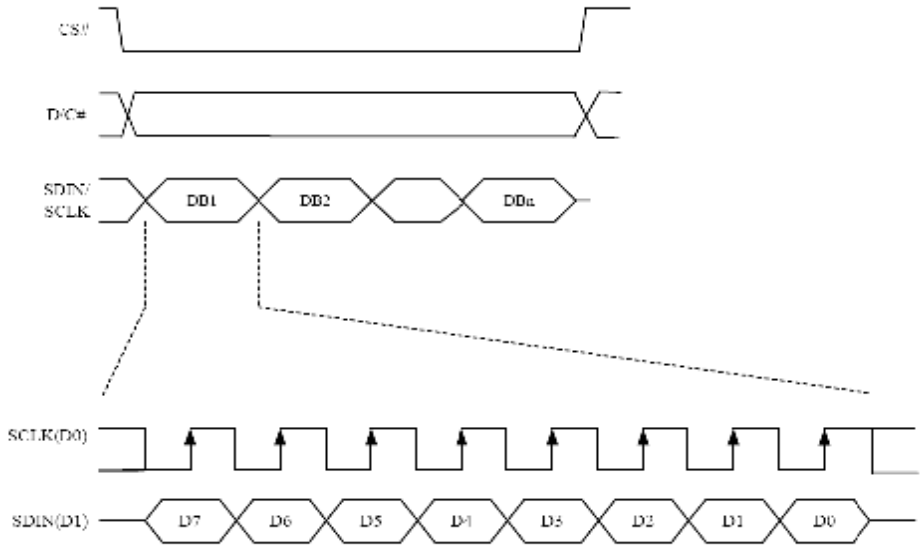
The serial interface consists of serial clock SCLK, serial data SDIN, D/C, /CS.In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W can be connected to an external ground.

Control pins of Serial interface

Function	E	R/W	/CS	D/C
Write command	Tie Low	Tie Low	L	L
Write data	Tie Low	Tie Low	L	H

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ...D0. A0 is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock. Under serial mode, only write operations are allowed.

Write procedure in SPI mode



4.4 MCU I2C Interface

The I2C communication interface consists of slave address bit SA0, I2C-bus data signal SDA(SDAOUT/D2 for output and SDAIN/D1 for input) and I2C-bus clock signal SCL (D0). Both thedata and clock signals must be connected to pull-up resistors. /RES is used for the initialization of device.

a) Slave address bit (SA0)

SSD1305 has to recognize the slave address before transmitting or receiving any information by the I2C-bus. The device will respond to the slave address following by the slave address bit("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

b7	b6	b5	b4	b3	b2	b1	b0
0	1	1	1	1	0	SA0	R/W

" SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1305. DC pin acts as SA0 for slave address selection. " R/W" bit is used to determine the operation mode of the I2C-bus interface. R/W=1, it is in read mode. R/W=0, it is in write mode.

b) I2C-bus data signal (SDA) SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

" SDAIN" and "SDAOUT" are tied together and serve as SDA. The "SDAIN" pin must be connected to act as SDA. The "SDAOUT" pin may be disconnected. When "SDAOUT" pin is disconnected, the acknowledgement signal will be ignored in the I2C-bus.

b) I2C-bus clock signal (SCL)

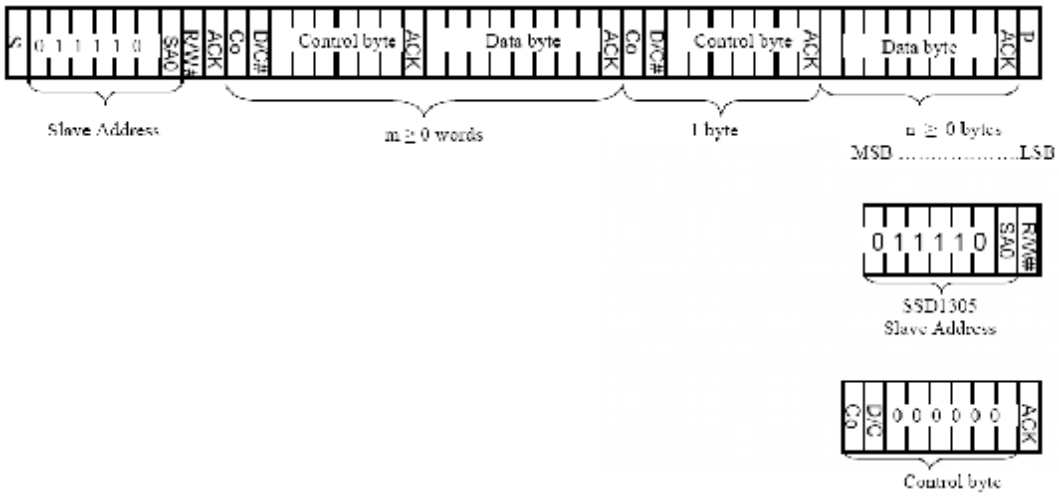
The transmission of information in the I2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

4.4.1 I2C-Bus Write Data

The I2C-bus interface gives access to write data and command into the device. Please refer to the following Figure for the write mode of I2C-bus in chronological order.

I2C-bus data format

Write mode



Note: Co – Continuation bit
D/C# - Data / Command Selection bit
ACK – Acknowledgement
SA0 – Slave address bit
R/W# - Read/Write Selection bit
S – Start Condition / P – Stop Condition

4.4.2 Write mode for I2C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in the followng Figure (1). The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1305, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (DC pin acts as SA0).
3) The write mode is established by setting the R/W bit to logic “0”.
4) An acknowledgement signal will be generated after receiving one byte of data,including the slave address and the R/W bit. Please refer to the following Figure (2) for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and A0 bits following by six “0” ‘s.
   a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
   b. The A0 bit determines the next data byte is acted as a command or a data. If the A0 bit is set to logic “0”, it defines the following data byte as a command. If the A0 bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure (1). The stop condition is established by

pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

Figure (1): Definition of the Start and Stop Condition

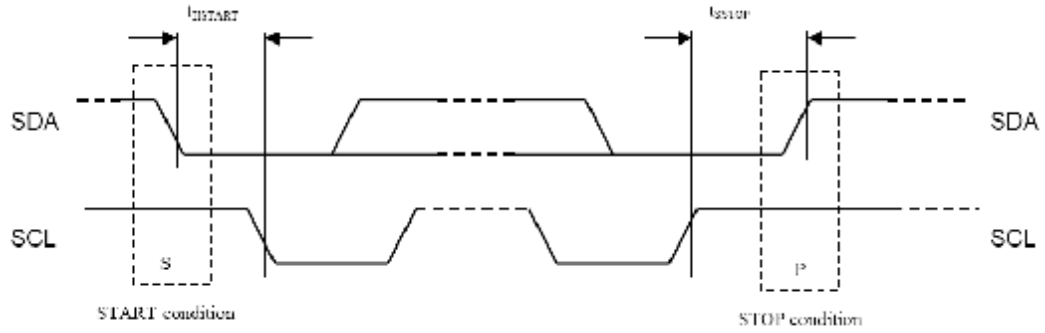
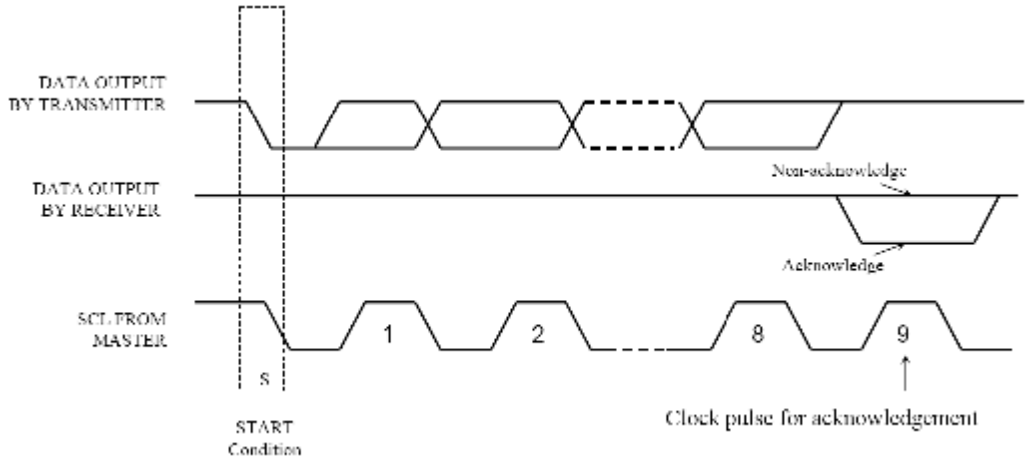


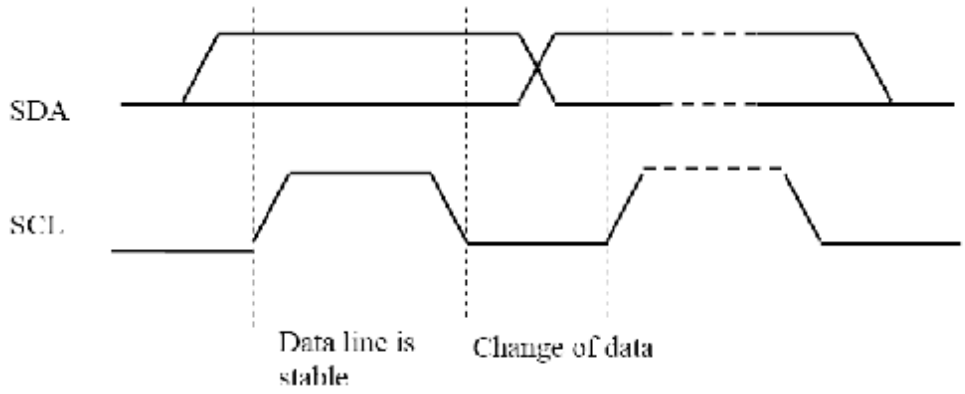
Figure (2):Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the “HIGH” period of the clock pulse. Please refer to the Figure (3) for graphical representations.Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure (3):Definition of the data transfer condition



4.5 Command Decoder

Refer to the Technical Manual for the SSD1305.

4.6 FR synchronization

Refer to the Technical Manual for the SSD1305.

4.7 Reset Circuit

When /RES input is low, the chip is initialized with the following status:

1. Display is OFF.
2. 132 x 64 MUX Display Mode.
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h).
4. Shift register data clear in serial interface.
5. Display start line is set at display RAM address 0.
6. Column address counter is set at 0.
7. Normal scan direction of the COM outputs.
8. Contrast control register is set at 80h.
9. Normal display mode (Equivalent to A4h command).

5. Reliability

5.1 Contents of Reliability Tests

ITEM	CONDITIONS		CRITERIA
High Temperature Operation	+85°C	t.b.d.	The operational functions work
Low Temperature Operation	-40°C	t.b.d.	
High Temperature Storage	+90°C	t.b.d.	
Low Temperature Storage	-45°C	t.b.d.	
High Temperature/Humidity Operation	+60°C	t.b.d.	
Thermal Shock	-40°C to +90°C	t.b.d.	

The samples used for the above tests do not include polarizer.
The moisture condensation is observed during tests.

5.2 Lifetime

End of lifetime is specified as 50% of initial brightness.

The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

PARAMETER	Min.	Max.	UNIT	CONDITIONS
Operating Lifetime	50.000	-	Hrs.	80cd/m2, 50% Checkerboard
Storage Lifetime	100.000	-	Hrs.	Ta~25°C, 50% RH

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23+/-5℃; 55+/-15%RH.

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature: 23+/-5℃
Humidity: 55+/-15%RH
Fluorescent Lamp: 30W
Distance between the Panel & Lamp: >=50 cm Distance
between the Panel & Eyes of the Inspector >=30 cm Finger glove

(or finger cover) must be worn by the inspector. Inspection table or jig must be anti-electrostatic.

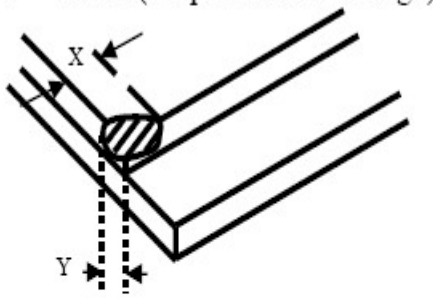
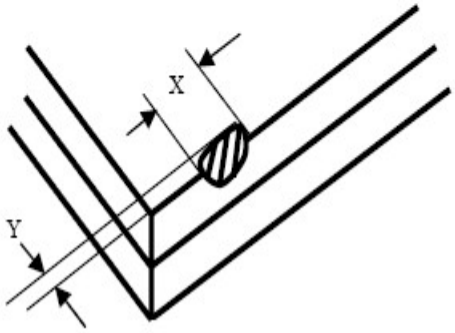
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

6.3 Criteria & Acceptable Quality Level

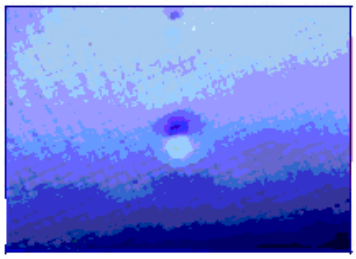
Partition	AQL	Definition
Major	0.61	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge)  

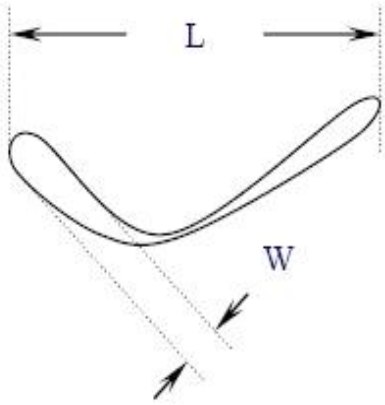
6.3.2 Cosmetic Check (Display Off) in Active Area

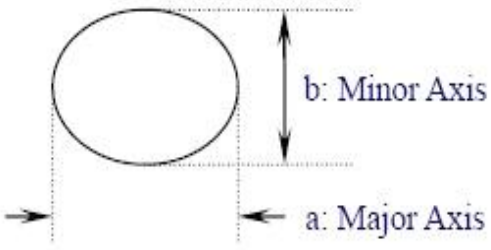
It is recommended to execute in clear room environment (class 10K) if actual in necessary.

Check Item	Classification	Criteria
Any Dirt & Scratch on Protective Film	Acceptable	Ignore for Any
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore
		W ≤ 0.1 Ignore W > 0.1, L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Spot-Shape Defect (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 <Φ ≤ 0.25 n ≤ 1 0.25 <Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not allowable

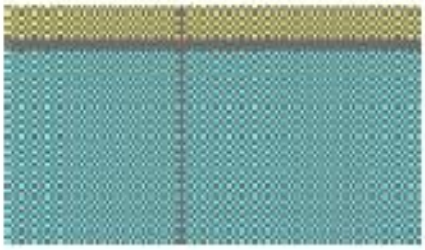
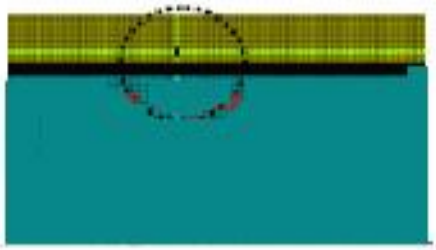
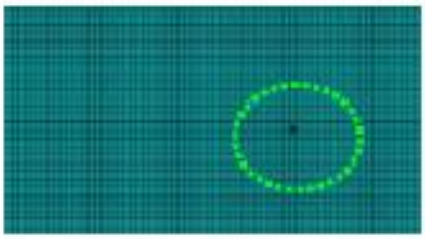
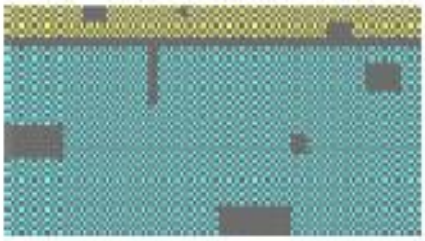
* Protective film should not be tear off when cosmetic chech.

** Definition of W & L & ϕ (Unit: mm): ϕ=(a+b)/2





6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7. Precautions When Using These OLED Display Modules

7.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OLED display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OLED display module is soft and easily scratched. Please be careful when handling the OLED display module.
5) When the surface of the polarizer of the OLED display module has soil,clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

   Also, pay attention that the following liquid and solvent may spoil the polarizer
   * Water
   * Ketone
   * Aromatic Solvents
6) When installing the OLED display module, be careful not to apply twisting stress or deflection stress to the OLED display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.
7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OLED display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OLED display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OLED display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OLED display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OLED display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

7.2 Storage Precautions

1) When storing OLED display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps.and, also, avoiding high temperature and high humidity environment or low temperature (less than 0 ° C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Topwin International CO., LTD) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OLED display module, when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

7.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OLED display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OLED display module, fasten the external plastic housing section.
7) If power supply to the OLED display module is forcibly shut down by such errors as taking out the main battery while the OLED display panel is in operation, we cannot guarantee the quality of this OLED display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSD1331
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

7.4 Precautions when disposing of the OLED display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OLED display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

7.5 Other Precautions

1) When an OLED display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OLED display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OLED display modules.
   * Pins and electrodes
   * Pattern layouts such as the COF
3) With this OLED display module, the OLED driver is being exposed.
   Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently,
   if this OLED driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OLED driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OLED driver may be shielded from light during the inspection processes.
4) Although this OLED display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

8. Appendixes

8.1 Display-module Software Initial Setting

```
Write_Command(0xae); /* set display off */
Write_Command(0x02); /* set  lower column start address */
Write_Command(0x10); /* set  higher column start address */
Write_Command(0x40); /* set  display start line */
Write_Command(0x2E);
Write_Command(0x81); /* set contrast control */
Write_Command(0x32);
Write_Command(0x82);
Write_Command(0x80);
Write_Command(0xa1); /* set segment remap */
Write_Command(0xa6); /* set normal display */
Write_Command(0xa8); /* set multiplex ratio */
Write_Command(0x3f); /* 1/64 */
Write_Command(0xad); /* master configuration */
Write_Command(0x8e); /* external vcc supply */
Write_Command(0xc8); /* set com scan direction */
Write_Command(0xd3); /* set  display offset */
Write_Command(0x40);
Write_Command(0xd5); /* set display clock divide/oscillator frequency */
Write_Command(0xf0);
Write_Command(0xD8); /*set area color mode off */
Write_Command(0x05);
Write_Command(0xD9); Write_Command(0xF1);
Write_Command(0xda); /* set com pin configuartion */
Write_Command(0x12);
Write_Command(0x91);
Write_Command(0x3F);
Write_Command(0x3F);
Write_Command(0x3F);
Write_Command(0x3F);
Write_Command(0xaf); /* set display on */
```