

Display Elektronik GmbH

# DATA SHEET

***TFT MODULE***

**DEM 240320K TMH-PW-N  
(C-TOUCH)**

**2,8" TFT + PCT**

Product Specification

Ver.: 0

12.06.2017

**Revision History**

<b>Revision</b>	<b>Date</b>	<b>Detail</b>	<b>Remarks</b>
0	12.06.2017	Initial Release	-

**Table of Contents**

1. General Description .....	4
2. Module Parameter .....	4
3. Absolute Maximum Ratings .....	4
4. DC Characteristics .....	5
5. Backlight Characteristic .....	5
5.1. Backlight Characteristics.....	5
5.2. Backlighting circuit .....	5
6. Touch Screen Panel Specifications.....	6
7. Optical Characteristics .....	7
7.1. Optical Characteristics .....	7
7.2. Definition of Response Time .....	7
7.3. Definition of Contrast Ratio .....	8
7.4. Definition of Viewing Angles.....	8
7.5. Definition of Color Appearance .....	9
7.6. Definition of Surface Luminance, Uniformity and Transmittance.....	9
8. Block Diagram and Power Supply .....	10
9. Interface Pins Definition .....	11
10. AC Characteristics .....	14
11. Reset Timing .....	21
12. Quality Assurance .....	22
12.1. Purpose .....	22
12.2. Standard for Quality Test.....	22
12.3. Nonconforming Analysis & Disposition .....	22
12.4. Agreement Items.....	22
12.5. Standard of the Product Visual Inspection .....	23
12.6. Inspection Specification .....	23
12.7. Classification of Defects.....	30
12.8. Identification/marketing criteria .....	30
12.9. Packaging .....	30
13. Reliability Specification .....	31
14. Precautions and Warranty .....	32
14.1 Safety.....	32
14.2. Handling .....	32
14.3. Storage.....	32
14.4. Metal Pin (Apply to Products with Metal Pins) .....	32
14.5. Operation .....	33
14.6. Static Electricity .....	33
14.7. Limited Warranty .....	33
15. Outline Drawing .....	34

**1. General Description**

The specification is a transmissive type color active matrix liquid crystal display (LCD) which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT-LCD panel, driver Ics, a touch panel and a backlight unit. This TFT Module is having an universal interface pin layout to access all relevant interfaces of the TFT Driver IC. It allows to be flexible in case of TFT driver IC changes.

**2. Module Parameter**

Features	Details	Unit
Display Size (Diagonal)	2.8"	-
LCD Type	TN TFT	-
Display Mode	Transmissive / Normally White	-
Resolution	240 x RGB x 320	Pixels
View Direction	6 O'clock	Best Image
Gray Scale Inversion Direction	12 clock	-
Module Outline	56.00 x 75.20 x 4.40 ( Note1 )	mm
Active Area	43.20 x 57.60	mm
Pixel Size	0.180 x 0.180	mm
Pixel Arrangement	R.G.B. Vertical Stripe	-
Polarizer Surface Treatment	Anti-Glare	-
Display Colors	262k	-
Interface	8/9/16/18-MPU-Parallel-Interface or 3-Wire 9-Bit-Interface + RGB Interface or 4-Wire 8-Bit-Interface + RGB Interface	-
With or without Touch Panel	With Projective Capacitive Touch	-
Driver IC	ILI9341V (Ilitek)	-
Operating Temperature	-20°C to +70°C	°C
Storage Temperature	-30°C to +80°C	°C
Weight	28	g

Note 1: Exclusive hooks, posts, FFC/FPC tail etc.

**3. Absolute Maximum Ratings**

$V_{SS}=0V$ ,  $T_a=25^{\circ}C$

Item	Symbol	Min.	Max.	Unit
Supply Voltage	Logic	-0.3	4.6	V
	Analog	-0.3	4.6	V
Storage Temperature	$T_{STG}$	-30	+80	°C
Operating Temperature	$T_{OP}$	-20	+70	°C

Note 1: If  $T_a$  below 50°C, the maximal humidity is 90%RH, if  $T_a$  over 50°C, absolute humidity should be less than 60%RH.

Note 2: The response time will be extremely slow when the operating temperature is around -10°C, and the back ground will become darker at high temperature operating.

**4. DC Characteristics**

Item		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Logic	IOVCC	1.65	1.8/2.8	3.3	V
	Analog	VCC	2.4	2.8	3.3	V
Logic Low input voltage		V <sub>IL</sub>	GND	-	0.3*IOVCC	V
Logic High input voltage		V <sub>IH</sub>	0.7*IOVCC	-	IOVCC	V
Logic Low output voltage		V <sub>OL</sub>	GND	-	0.2*IOVCC	V
Logic High output voltage		V <sub>OH</sub>	0.8*IOVCC	-	IOVCC	V
Current Consumption All Black	Logic	I <sub>CC+</sub> I <sub>IN</sub>	-	10	-	mA
	Analog					

**5. Backlight Characteristic**

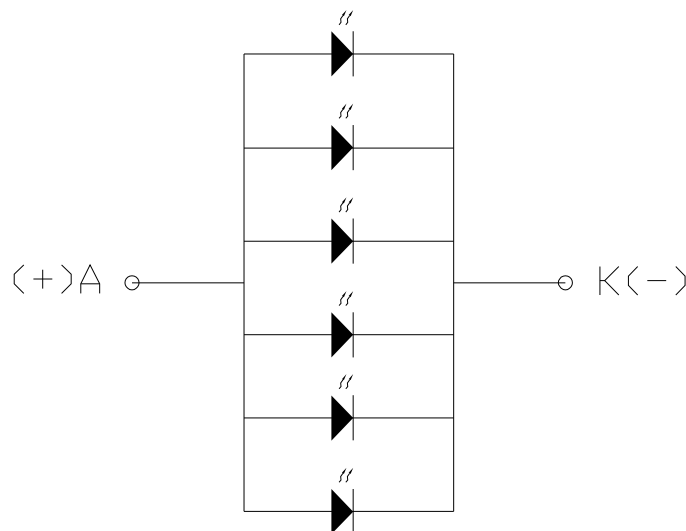
**5.1. Backlight Characteristics**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward Voltage	V <sub>F</sub>	T <sub>a</sub> =25 °C, I <sub>F</sub> =20mA/LED	2.9	3.2	3.4	V
Forward Current	I <sub>F</sub>	T <sub>a</sub> =25 °C, V <sub>F</sub> =3.2V/LED	-	120	-	mA
Power Dissipation	P <sub>D</sub>		-	384	-	mW
LED Lifetime (25°C)	-	-	(20,000)	(30,000)	-	Hr
Uniformity	Avg		-	80	-	%
Drive Method	Constant Current					
LED Configuration	6 White LEDs in parallel					

Note: LED Lifetime defined as follows: The final brightness is at 50% of original brightness.

The environmental conducted under ambient air flow, at T<sub>a</sub>=25°C±2 °C, 60%RH±5%, I<sub>F</sub>=20mA/LED.

**5.2. Backlighting Circuit**



## **6. Touch Screen Panel Specifications**

### **Technical Parameters:**

1. Cover Glass+LOCA+ITO GLASS+FPC  
ITO Glass: T=0.55mm  
Cover Glass: 0.7mm  
Lead Line: FPC  
IC Model: FT5336 (Focaltech)
2. Operation Voltage: 2.8V-3.3 V
3. Transmittance: ≥85%
4. Surface Hardness: ≥6H
5. Operation Environment: -20°C to +70°C
6. Storage Environment: -30°C to +80°C

7. Optical Characteristics

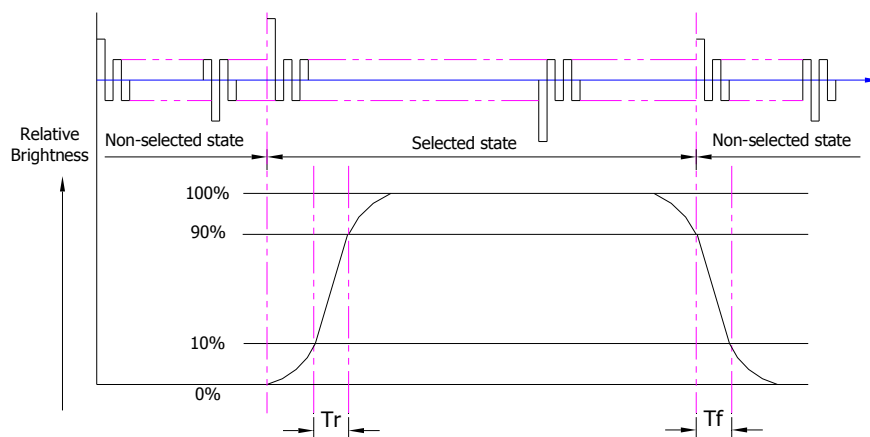
7.1. Optical Characteristics

Ta=25°C, V<sub>DD</sub>=2.8V, TN LC+ Polarizer

	Item	Symbol	Condition	Specification			Unit	
				Min.	Typ.	Max.		
Backlight On (Transmissive Mode)	Luminance on TFT(I <sub>f</sub> =20mA/LED)	Lv	Normally viewing angle θ <sub>x</sub> = φ <sub>y</sub> = 0°	300	380	-	cd/m <sup>2</sup>	
	Contrast Ratio(See 7.3)	CR		400	500	-		
	Response Time (See 7.2)	T <sub>R</sub> +T <sub>F</sub>		-	16	32	ms	
	Chromaticity Transmissive (See 7.5)	Red	X <sub>R</sub>	Center CR≥10	0.567	0.617	0.667	
			Y <sub>R</sub>		0.306	0.356	0.406	
		Green	X <sub>G</sub>		0.238	0.288	0.338	
			Y <sub>G</sub>		0.542	0.592	0.642	
		Blue	X <sub>B</sub>		0.094	0.144	0.194	
			Y <sub>B</sub>		0.030	0.080	0.130	
	White	X <sub>W</sub>	0.223	0.273	0.323			
		Y <sub>W</sub>	0.253	0.303	0.353			
	Viewing Angle (See 7.4)	Horizontal	θ <sub>x+</sub>	Center CR≥10	50	60	-	Deg.
			θ <sub>x-</sub>		50	60	-	
		Vertical	φ <sub>y+</sub>		50	60	-	
φ <sub>y-</sub>			40		50	-		
NTSC Ratio(Gamut)				-	60	-	%	

7.2. Definition of Response Time

7.2.1. Normally Black Type (Negative)

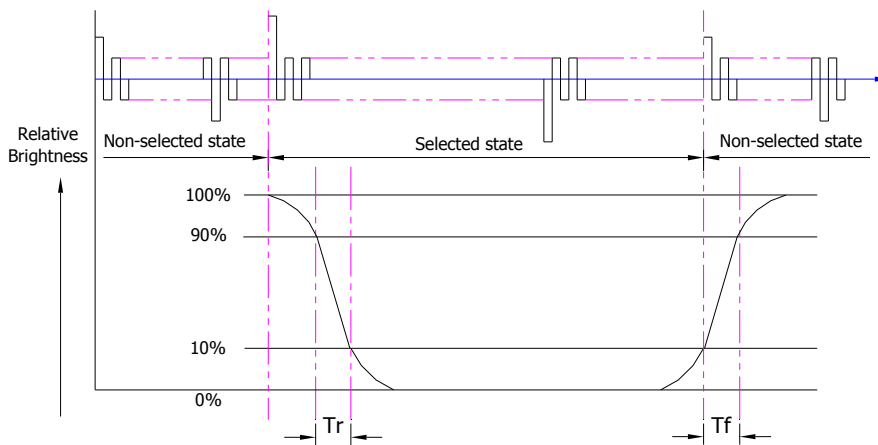


Tr is the time it takes to change from non-selected stage with relative luminance 10% to selected state with relative luminance 90%;

Tf is the time it takes to change from selected state with relative luminance 90% to non-selected state with relative luminance 10%.

Note: Measuring machine: LCD-5100

**7.2.2. Normally White Type (Positive)**



Tr is the time it takes to change from non-selected stage with relative luminance 90% to selected state with relative luminance 10%;

Tf is the time it takes to change from selected state with relative luminance 10% to non-selected state with relative luminance 90%;

Note: Measuring machine: LCD-5100 or EQUI

**7.3. Definition of Contrast Ratio**

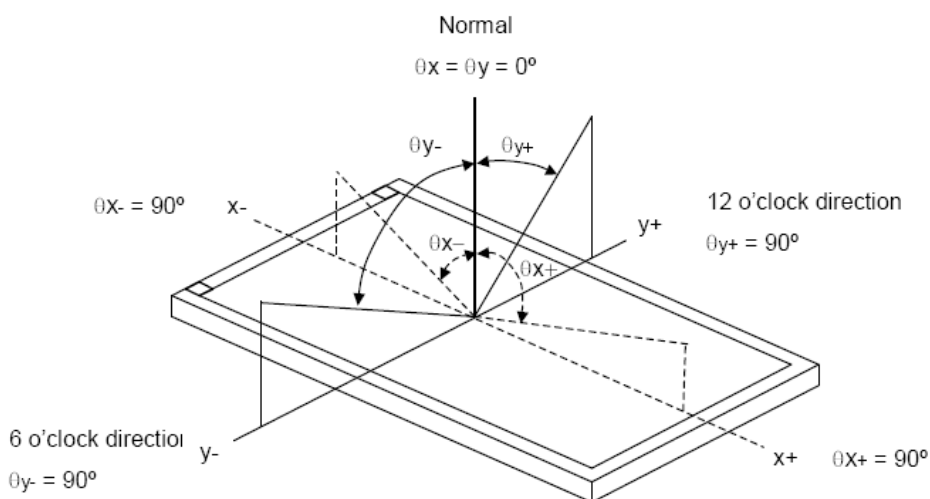
Contrast is measured perpendicular to display surface in reflective and transmissive mode.

The measurement condition is:

Measuring Equipment	Eldim or Equivalent
Measuring Point Diameter	3mm//1mm
Measuring Point Location	Active Area centre point
Test pattern	A: All Pixels white B: All Pixel black
Contrast setting	Maximum

Definitions: CR (Contrast) = Luminance of White Pixel / Luminance of Black Pixel

**7.4. Definition of Viewing Angles**



Measuring machine: LCD-5100 or EQUI

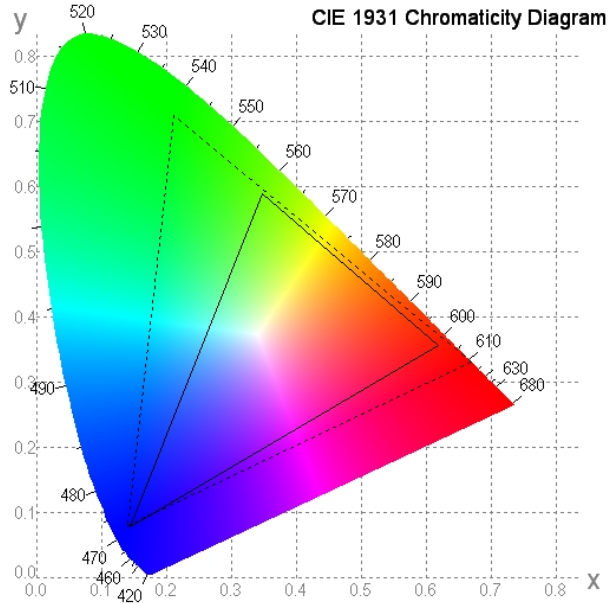


**7.5. Definition of Color Appearance**

R,G,B and W are defined by (x, y) on the IE chromaticity diagram

NTSC=area of RGB triangle/area of NTSC triangleX100%

Measuring picture: Red, Green, Blue and White (Measuring machine: BM-7)



**7.6. Definition of Surface Luminance, Uniformity and Transmittance**

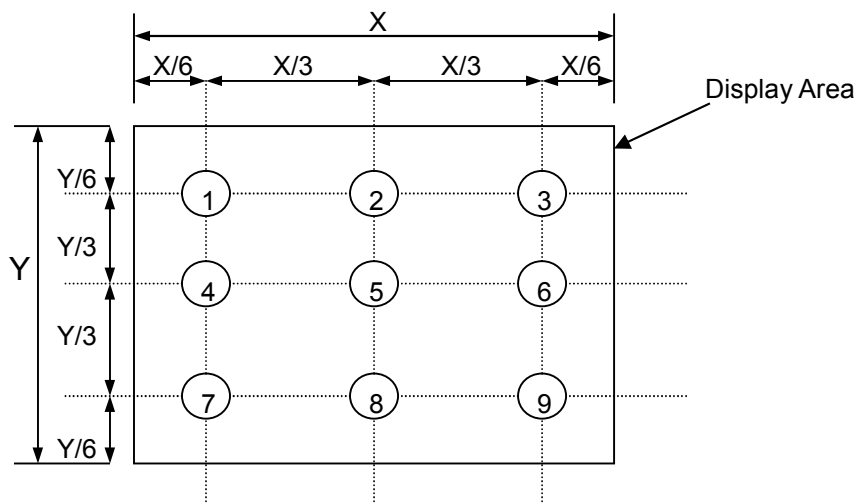
Using the transmissive mode measurement approach, measure the white screen luminance of the display panel and backlight.

7.6.1. Surface Luminance:  $L_v = \text{average} (L_{P1}:L_{P9})$

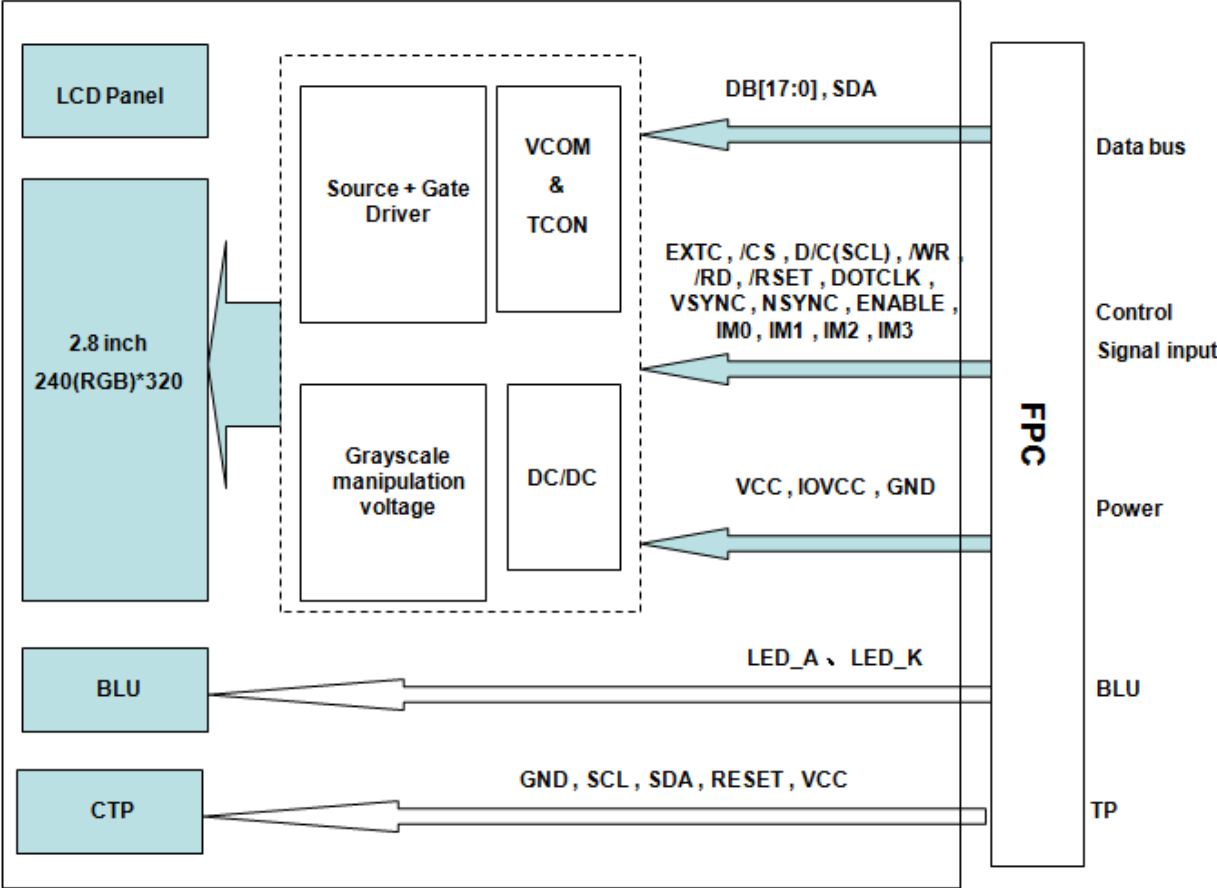
7.6.2. Uniformity =  $\text{Minimal} (L_{P1}:L_{P9}) / \text{Maximal} (L_{P1}:L_{P9}) * 100\%$

7.6.3. Transmittance =  $L_v \text{ on LCD} / L_v \text{ on Backlight} * 100\%$

Note: Measuring machine: BM-7



8. Block Diagram and Power Supply



## 9. Interface Pins Definition

### 9.1 TFT PIN:

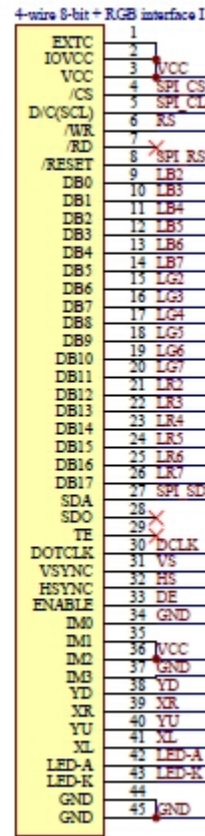
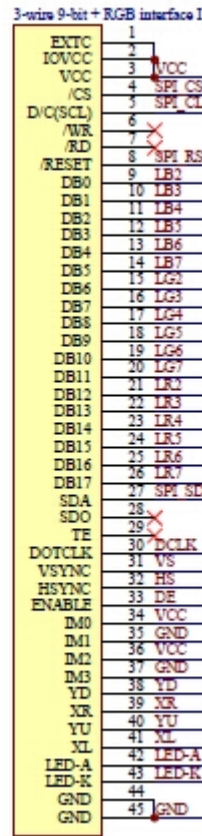
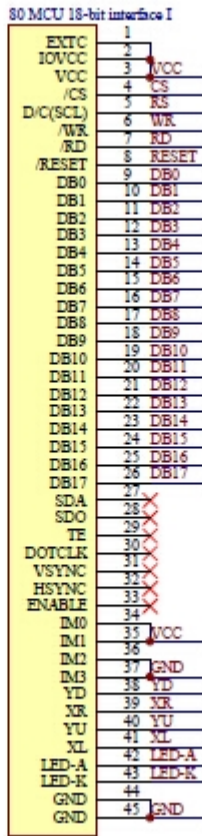
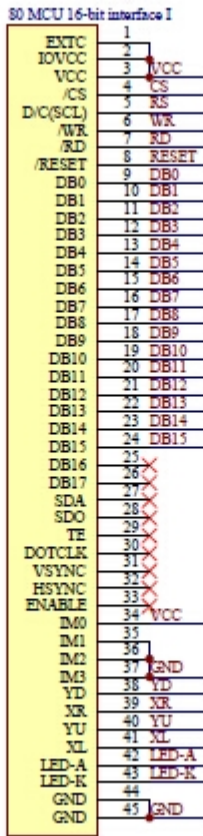
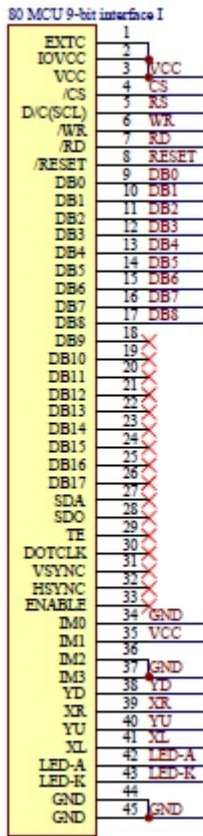
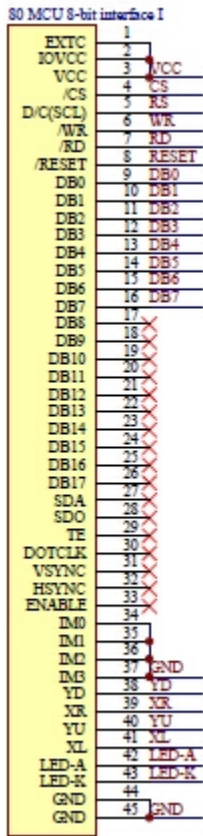
No.	Symbol	Function
1	EXTC	Extended command set enable. High: extended command set is accepted. EXTC must be set "H" to read/write extended registers.
2	IOVCC(1.8/2.8V)	Digital Supply Power.
3	VCC(2.8V)	Analog Supply Power.
4	/CS	Chip Select Signal (Low: active).
5	D/C(SCL)	D/C: Data/Commander Selection. SCL: Serial clock in 3-wire 9-bit/4-wire 8-bit serial data interface.
6	/WR	8080-system: Serves as Write Signal. 4-line system: Serves as the selector of command or parameter.
7	/RD	Read Signal.
8	/RESET	Reset Signal.
9	DB0	Data Bus.
10	DB1	Data Bus.
11	DB2	Data Bus.
12	DB3	Data Bus.
13	DB4	Data Bus.
14	DB5	Data Bus.
15	DB6	Data Bus.
16	DB7	Data Bus.
17	DB8	Data Bus.
18	DB9	Data Bus.
19	DB10	Data Bus.
20	DB11	Data Bus.
21	DB12	Data Bus.
22	DB13	Data Bus.
23	DB14	Data Bus.
24	DB15	Data Bus.
25	DB16	Data Bus.
26	DB17	Data Bus.
27	SDA	SPI interface input pin.
28	SDO	SPI interface output pin.
29	TE	Tearing effect output pin to synchronize MPU to frame writing, active by S/W command.
30	DOTCLK	Pixel clock signal in RGB I/F mode.
31	VSYNC	Vertical sync. Signal in RGB I/F mode.
32	HSYNC	Horizontal sync. Signal in RGB I/F mode.
33	ENABLE	Data enable signal in RGB I/F mode.

		IM3	IM2	IM1	IM0	MPU interface Mode	DB pin	
							Register	Gram
34 35 36 37	IM0 IM1 IM2 IM3	0	0	0	0	80 MCU 8-bit bus interface I	DB[7:0]	DB[7:0]
		0	0	0	1	80 MCU 16-bit bus interface I	DB[7:0]	DB[15:0]
		0	0	1	0	80 MCU 9-bit bus interface I	DB[7:0]	DB[8:0]
		0	0	1	1	80 MCU 18-bit bus interface I	DB[7:0]	DB[17:0]
		0	1	0	1	3-wire 9-bit data Serial interface I	SDA: in/out	
		0	1	1	0	4-wire 8-bit data Serial interface I	SDA: in/out	
		1	0	0	0	80 MCU 16-bit bus interface II	DB[8:1]	DB[8:1] DB[17:10]
		1	0	0	1	80 MCU 8-bit bus interface II	DB[17:10]	DB[17:10]
		1	0	1	0	80 MCU 18-bit bus interface II	DB[8:1]	DB[17:0]
		1	0	1	1	80 MCU 9-bit bus interface II	DB[17:10]	DB[17:9]
		1	1	0	1	3-wire 9-bit data Serial interface II	SDI: in SDO: out	
		1	1	1	0	4-wire 8-bit data Serial interface II	SDI: in SDO: out	
		38	NC	NC				
39	NC	NC						
40	NC	NC						
41	NC	NC						
42	LED-A	LED Anode.						
43	LED-K	LED Cathode.						
44	GND	Ground.						
45	GND	Ground.						

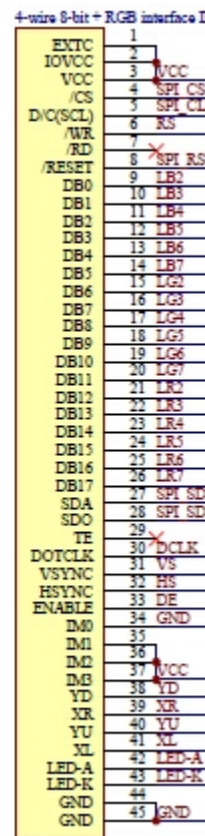
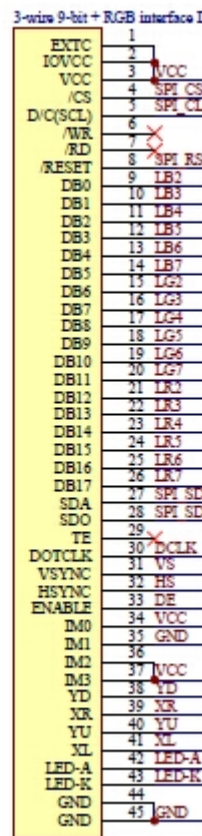
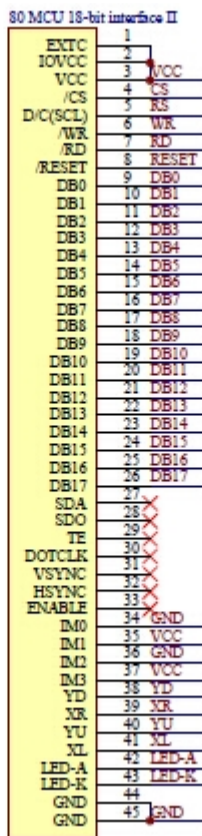
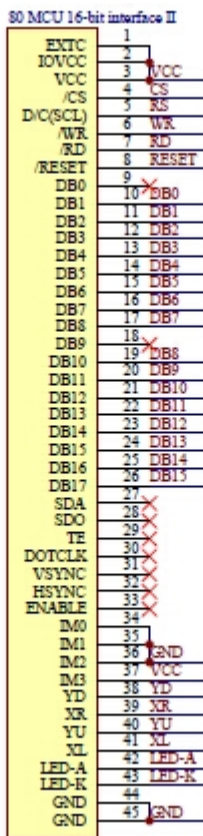
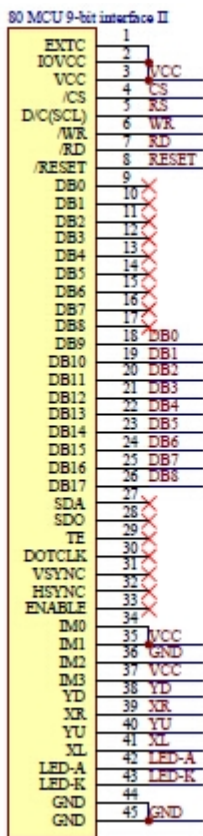
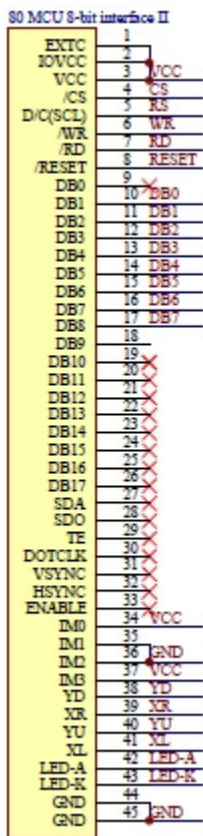
9.2 CTP PIN:

No.	Symbol	Function
1	GND	Ground
2	SCL	Clock
3	SDA	Data
4	INT	Interrupt
5	RESET	Reset
6	VCC	Power supply

80 MCU Interface I



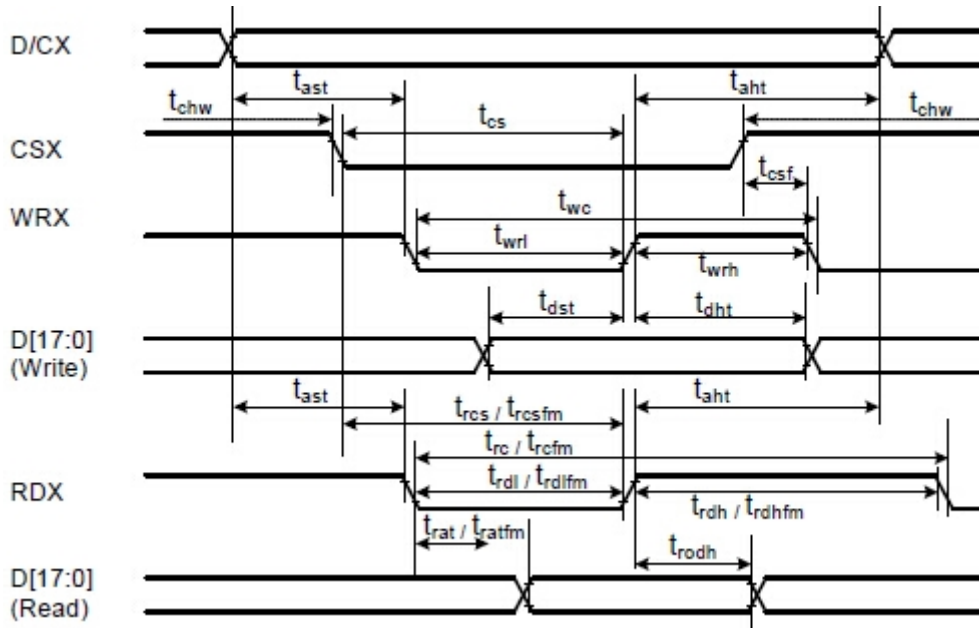
80 MCU Interface II





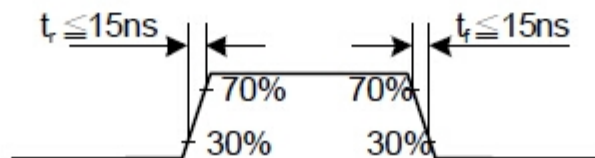
10. AC Characteristics

10.1 Display Parallel 18/16/9/8-Bit Parallel Interface Timing Characteristics (8080-I system)

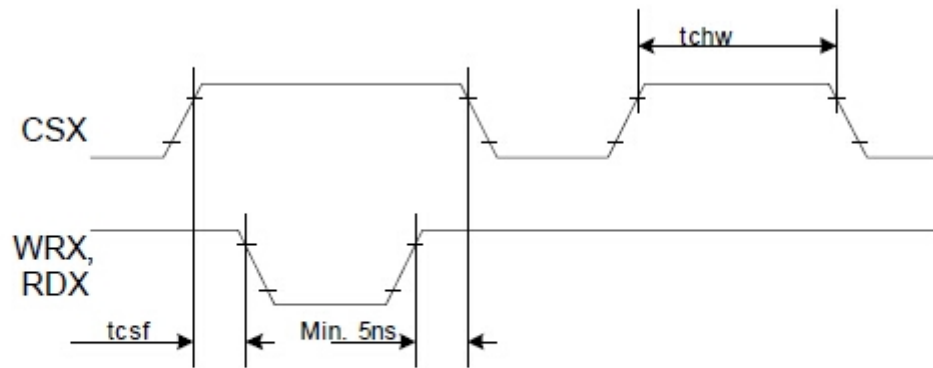


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note:  $T_a = -30$  to  $70$  °C,  $V_{DDI}=1.65V$  to  $3.3V$ ,  $V_{CI}=2.5V$  to  $3.3V$ ,  $V_{SS}=0V$

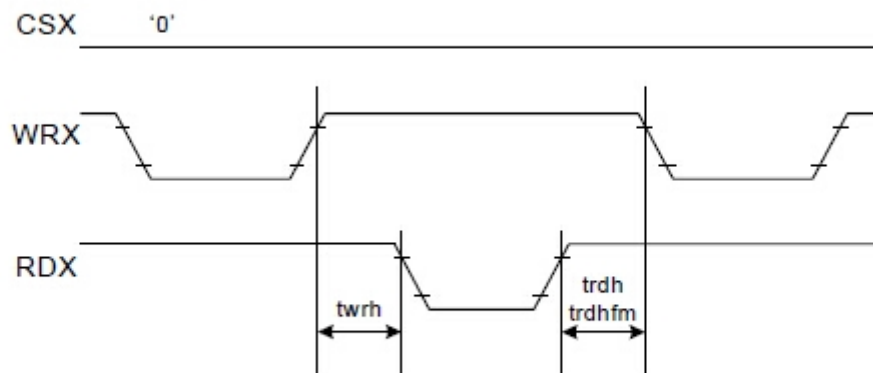


CSX timings :



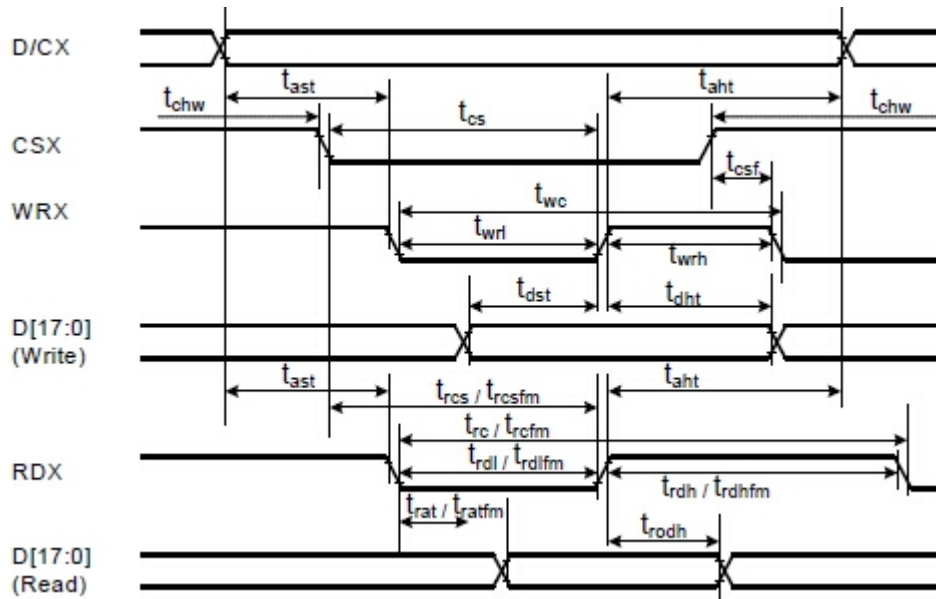
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



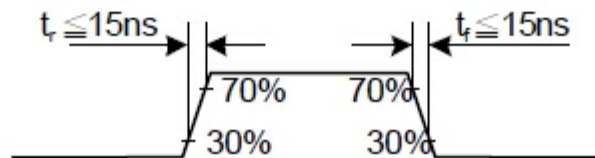
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

9.2 Display Parallel 18/16/9/8-Bit Interface Timing Characteristics (8080-II system)



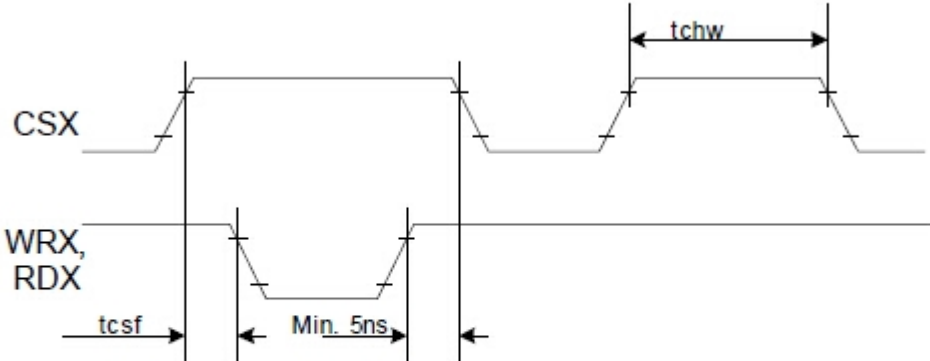
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t <sub>ast</sub>	Address setup time	0	-	ns	
	t <sub>ah</sub>	Address hold time (Write/Read)	0	-	ns	
CSX	t <sub>chw</sub>	CSX "H" pulse width	0	-	ns	
	t <sub>cs</sub>	Chip Select setup time (Write)	15	-	ns	
	t <sub>rcs</sub>	Chip Select setup time (Read ID)	45	-	ns	
	t <sub>rcsfm</sub>	Chip Select setup time (Read FM)	355	-	ns	
WRX	t <sub>csf</sub>	Chip Select Wait time (Write/Read)	10	-	ns	
	t <sub>wc</sub>	Write cycle	66	-	ns	
	t <sub>wrh</sub>	Write Control pulse H duration	15	-	ns	
RDX (FM)	t <sub>wrl</sub>	Write Control pulse L duration	15	-	ns	
	t <sub>rcfm</sub>	Read Cycle (FM)	450	-	ns	
	t <sub>rdhfm</sub>	Read Control H duration (FM)	90	-	ns	
RDX (ID)	t <sub>rdlfm</sub>	Read Control L duration (FM)	355	-	ns	
	t <sub>rc</sub>	Read cycle (ID)	160	-	ns	
	t <sub>rdh</sub>	Read Control pulse H duration	90	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	t <sub>rdl</sub>	Read Control pulse L duration	45	-	ns	
	t <sub>dst</sub>	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t <sub>dht</sub>	Write data hold time	10	-	ns	
	t <sub>rat</sub>	Read access time	-	40	ns	
t <sub>ratfm</sub>	Read access time	-	340	ns		
	t <sub>rod</sub>	Read output disable time	20	80	ns	

Note: T<sub>a</sub> = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.



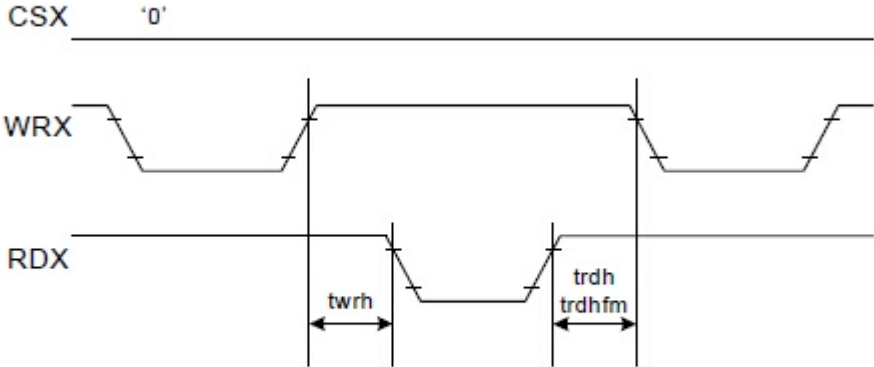


CSX timings :



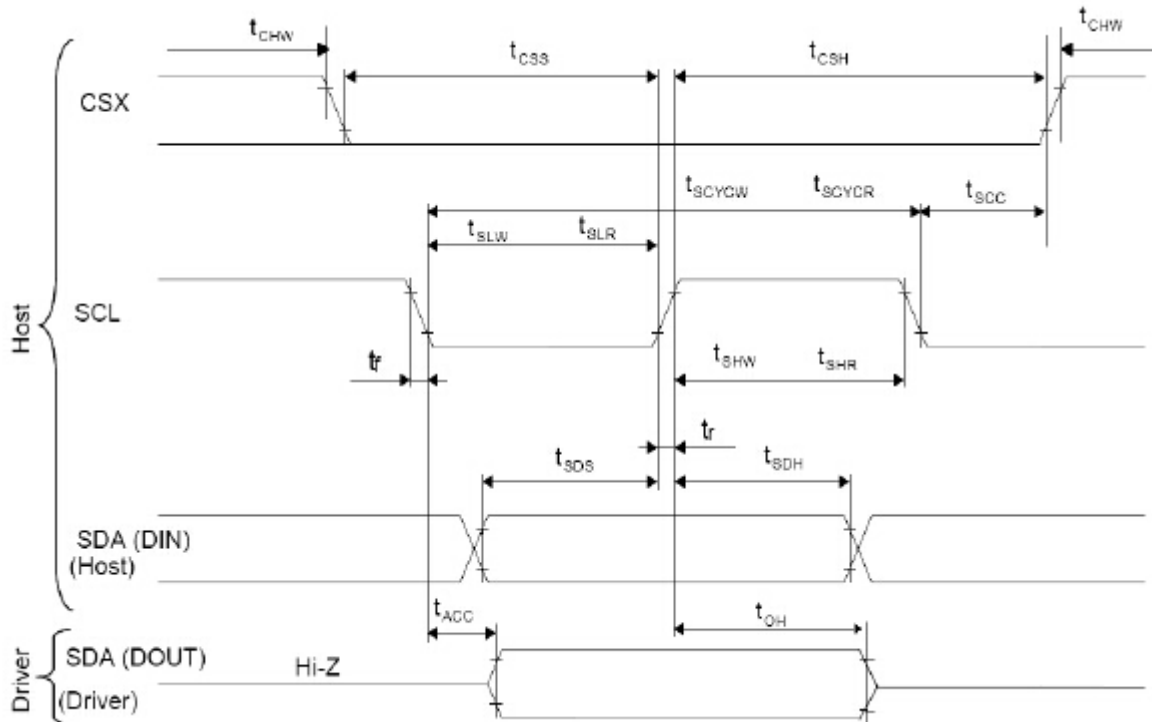
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



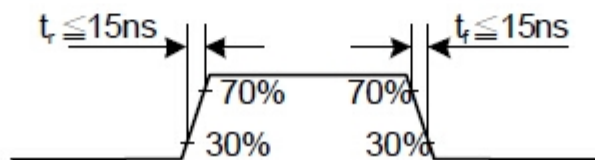
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

9.3 Display Serial Interface Timing Characteristics (3-Line SPI System)

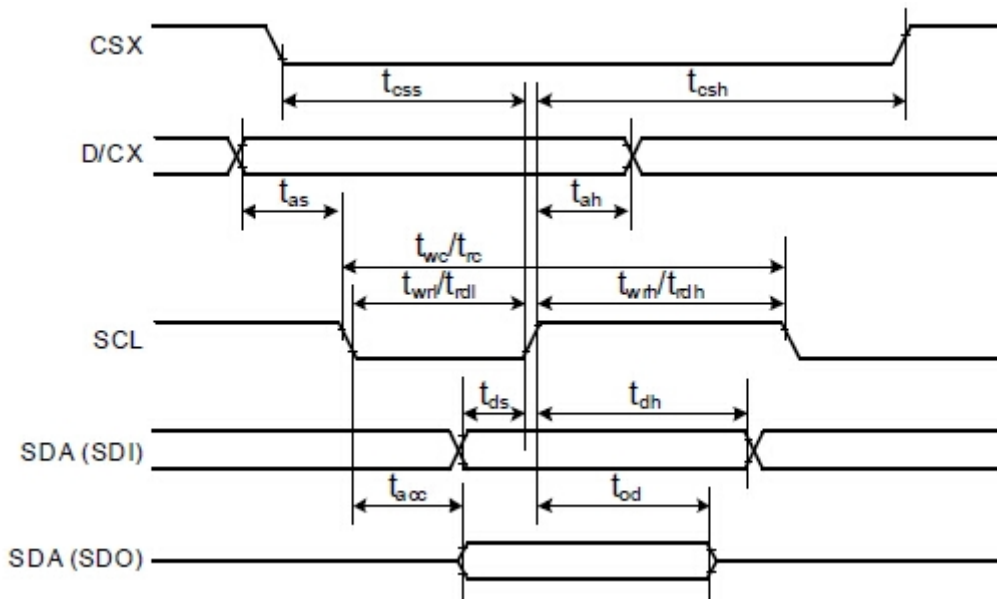


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tsc	SCL-CSX	20	-	ns	
	tch	CSX "H" Pulse Width	40	-	ns	
	tcs	CSX-SCL Time	60	-	ns	
	tcs		65	-	ns	

Note:  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DDI}=1.65\text{V to }3.3\text{V}$ ,  $V_{CI}=2.5\text{V to }3.3\text{V}$ ,  $AGND=VSS=0\text{V}$

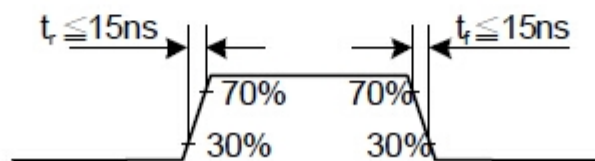


9.4 Display Serial Interface Timing Characteristics (4-Line SPI System)

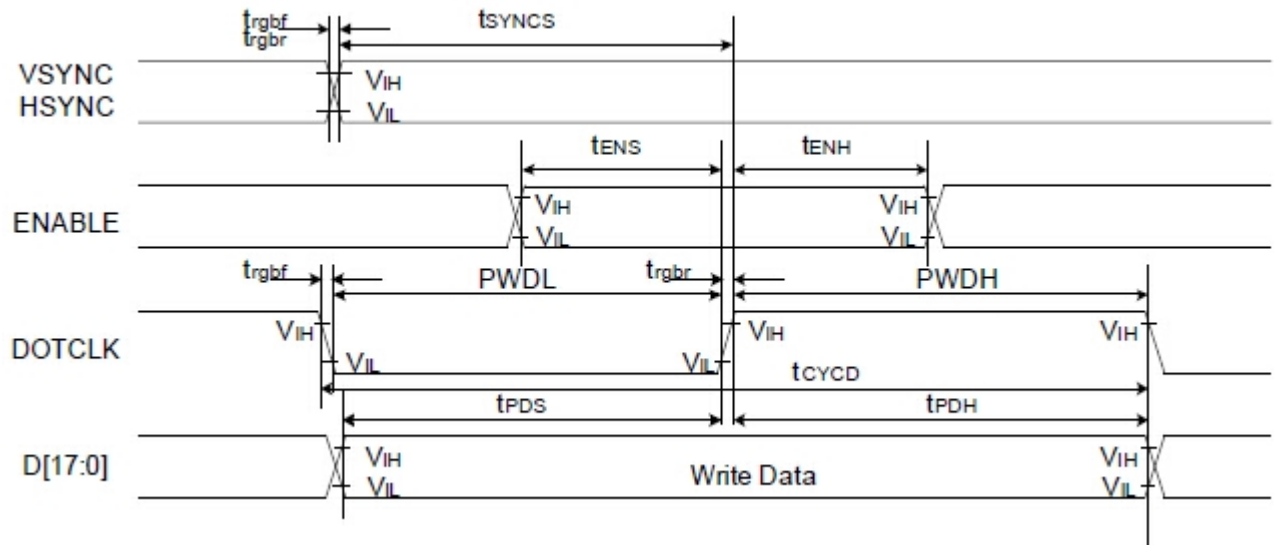


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	$t_{css}$	Chip select time (Write)	40	-	ns	
	$t_{csh}$	Chip select hold time (Read)	40	-	ns	
SCL	$t_{wc}$	Serial clock cycle (Write)	100	-	ns	
	$t_{wrh}$	SCL "H" pulse width (Write)	40	-	ns	
	$t_{wrl}$	SCL "L" pulse width (Write)	40	-	ns	
	$t_{rc}$	Serial clock cycle (Read)	150	-	ns	
	$t_{rdh}$	SCL "H" pulse width (Read)	60	-	ns	
	$t_{rdl}$	SCL "L" pulse width (Read)	60	-	ns	
D/CX	$t_{as}$	D/CX setup time	10	-		
	$t_{ah}$	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	$t_{ds}$	Data setup time (Write)	30	-	ns	
	$t_{dh}$	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	$t_{acc}$	Access time (Read)	10	-	ns	For maximum CL=30pF
	$t_{od}$	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note:  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DDI}=1.65\text{V to }3.3\text{V}$ ,  $V_{CI}=2.5\text{V to }3.3\text{V}$ ,  $AGND=VSS=0\text{V}$

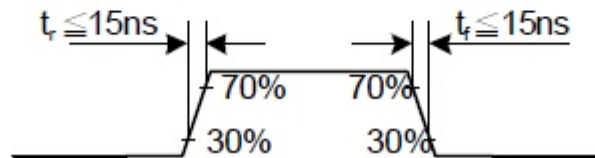


9.5 Parallel 18/16/6-Bit RGB Interface Timing Characteristics

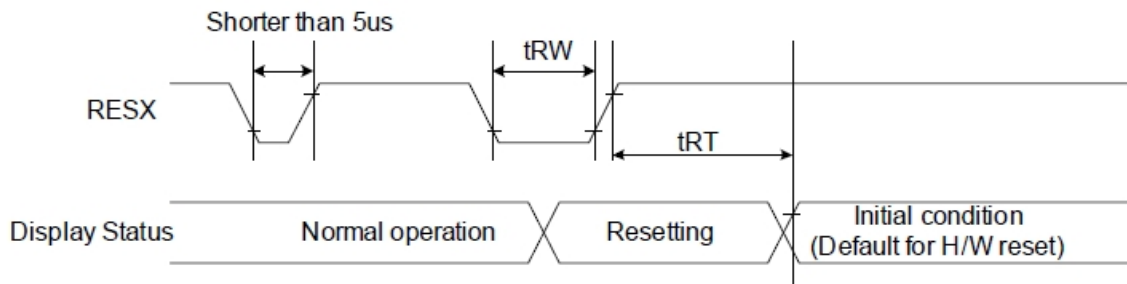


Signal	Symbol	Parameter	min	max	Unit	Description	
VSYNC / HSYNC	$t_{SYNCS}$	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode	
	$t_{SYNCH}$	VSYNC/HSYNC hold time	15	-	ns		
DE	$t_{ENS}$	DE setup time	15	-	ns		
	$t_{ENH}$	DE hold time	15	-	ns		
D[17:0]	$t_{POS}$	Data setup time	15	-	ns		
	$t_{PDH}$	Data hold time	15	-	ns		
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns		
	PWDL	DOTCLK low-level period	15	-	ns		
	$t_{CYCD}$	DOTCLK cycle time	100	-	ns		
	$t_{rgr}, t_{gr}$	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns		
VSYNC / HSYNC	$t_{SYNCS}$	VSYNC/HSYNC setup time	15	-	ns		6-bit bus RGB interface mode
	$t_{SYNCH}$	VSYNC/HSYNC hold time	15	-	ns		
DE	$t_{ENS}$	DE setup time	15	-	ns		
	$t_{ENH}$	DE hold time	15	-	ns		
D[17:0]	$t_{POS}$	Data setup time	15	-	ns		
	$t_{PDH}$	Data hold time	15	-	ns		
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns		
	PWDL	DOTCLK low-level pulse period	15	-	ns		
	$t_{CYCD}$	DOTCLK cycle time	50	-	ns		
	$t_{rgr}, t_{gr}$	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns		

Note:  $T_a = -30$  to  $70$  °C,  $V_{DDI}=1.65V$  to  $3.3V$ ,  $V_{CI}=2.5V$  to  $3.3V$ ,  $AGND=VSS=0V$



11. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

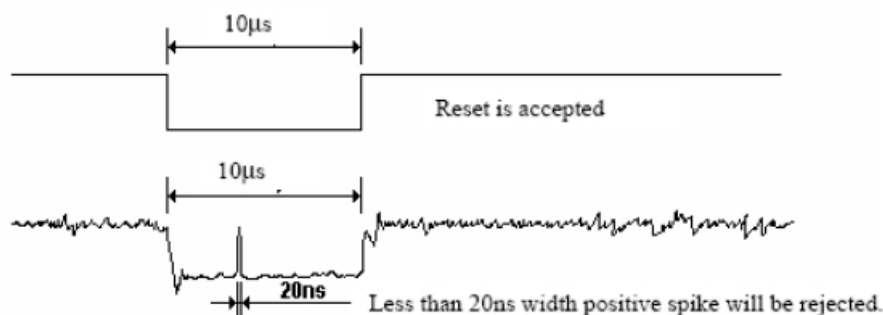
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

## **12. Quality Assurance**

### **12.1. Purpose**

This standard for Quality Assurance assures the quality of LCD module products supplied to customer.

### **12.2. Standard for Quality Test**

#### 12.2.1 Sampling Plan:

GB2828.1-2012

Single sampling, normal inspection.

#### 12.2.2 Sampling Criteria:

Visual inspection: AQL 1.5%

Electrical functional: AQL 0.65%.

#### 12.2.3 Reliability Test:

Detailed requirement refer to Reliability Test Specification.

### **12.3. Nonconforming Analysis & Disposition**

#### 12.3.1 Nonconforming analysis:

12.3.1.1 Customer should provide overall information of non-conforming sample for their complaints.

12.3.1.2 After receipt of detailed information from customer, the analysis of nonconforming parts usually should be finished in one week.

12.3.1.3 If cannot finish the analysis on time, customer will be notified with the progress status.

#### 12.3.2 Disposition of nonconforming:

12.3.2.1 Non-conforming product over PPM level will be replaced.

12.3.2.2 The cause of non-conformance will be analyzed. Corrective action will be discussed and implemented.

### **12.4. Agreement Items**

Shall negotiate with customer if the following situation occurs:

12.4.1 There is any discrepancy in standard of quality assurance.

12.4.2 Additional requirement to be added in product specification.

12.4.3 Any other special problem.

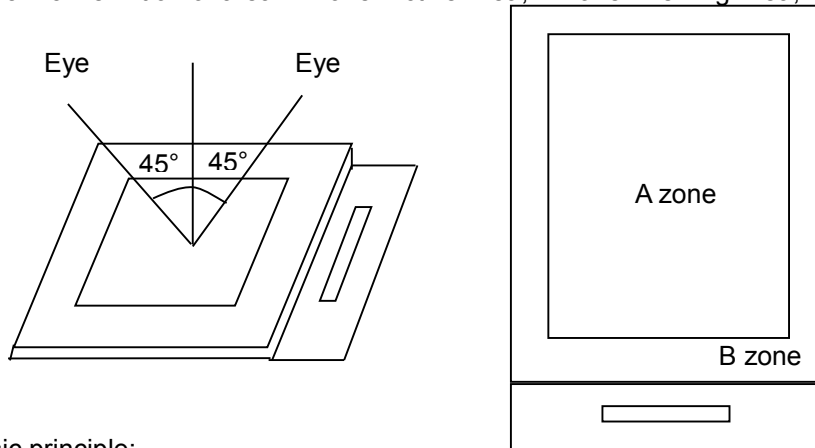
**12.5. Standard of the Product Visual Inspection**

12.5.1 Appearance inspection:

12.5.1.1 The inspection must be under illumination about 1000 – 1500 lx, and the distance of view must be at 30cm ± 2cm.

12.5.1.2 The viewing angle should be 45° from the vertical line without reflection light or follows customer's viewing angle specifications.

12.5.1.3 Definition of area: A Zone: Active Area, B Zone: Viewing Area,



12.5.2 Basic principle:

12.5.2.1 A set of sample to indicate the limit of acceptable quality level must be discussed by both us and customer when there is any dispute happened.

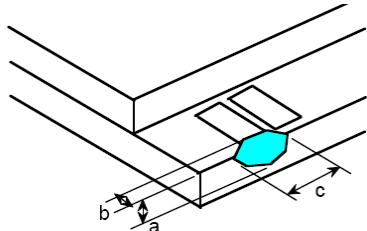
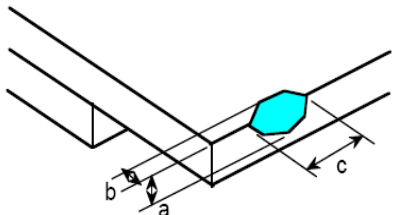
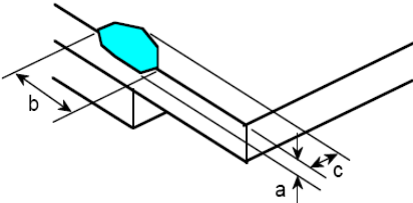
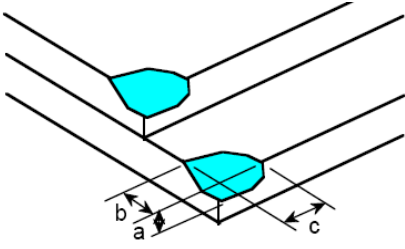
12.5.2.2 New item must be added on time when it is necessary.

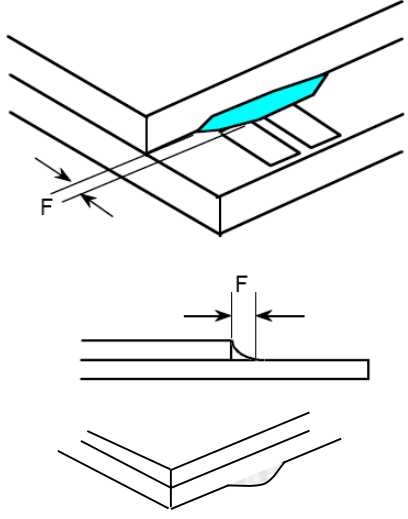
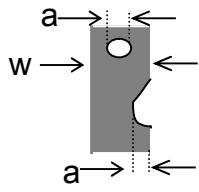
**12.6. Inspection Specification**

No.	Item	Criteria (Unit: mm)																			
01	Black / White spot Foreign material (Round type) Pinholes Stain Particles inside cell. (Minor defect)	$\phi = (a + b) / 2$ Distance between 2 defects should more than 3mm apart.	<table border="1"> <thead> <tr> <th>Size</th> <th>Area</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>\phi \leq 0.10</math></td> <td></td> <td>Ignore</td> </tr> <tr> <td><math>0.10 &lt; \phi \leq 0.15</math></td> <td></td> <td>2</td> </tr> <tr> <td><math>0.15 &lt; \phi \leq 0.25</math></td> <td></td> <td>1</td> </tr> <tr> <td><math>0.25 &lt; \phi</math></td> <td></td> <td>0</td> </tr> <tr> <td>Total</td> <td></td> <td>2 no include <math>\phi \leq 0.10</math></td> </tr> </tbody> </table>	Size	Area	Acc. Qty	$\phi \leq 0.10$		Ignore	$0.10 < \phi \leq 0.15$		2	$0.15 < \phi \leq 0.25$		1	$0.25 < \phi$		0	Total		2 no include $\phi \leq 0.10$
			Size	Area	Acc. Qty																
$\phi \leq 0.10$		Ignore																			
$0.10 < \phi \leq 0.15$		2																			
$0.15 < \phi \leq 0.25$		1																			
$0.25 < \phi$		0																			
Total		2 no include $\phi \leq 0.10$																			

02	Electrical Defect (Minor defect)	<table border="1"> <tr> <th></th> <th>Display Area</th> <th>Total</th> <th rowspan="3">Note1</th> </tr> <tr> <td>Bright dot</td> <td>0</td> <td>0</td> </tr> <tr> <td>Dark dot</td> <td><math>N \leq 2</math></td> <td><math>N \leq 2</math></td> </tr> <tr> <td>Total dot</td> <td><math>N \leq 2</math></td> <td><math>N \leq 2</math></td> <td rowspan="2">Note 2</td> </tr> <tr> <td>Mura</td> <td colspan="2">Not visible through 5% ND filters.</td> </tr> </table>		Display Area	Total	Note1	Bright dot	0	0	Dark dot	$N \leq 2$	$N \leq 2$	Total dot	$N \leq 2$	$N \leq 2$	Note 2	Mura	Not visible through 5% ND filters.	
			Display Area	Total	Note1														
Bright dot	0	0																	
Dark dot	$N \leq 2$	$N \leq 2$																	
Total dot	$N \leq 2$	$N \leq 2$	Note 2																
Mura	Not visible through 5% ND filters.																		
		<p>Remark:</p> <p>1. Bright dot caused by scratch and foreign object accords to item 1.</p>																	
03	Black and White line Scratch Foreign material (Line type) (Minor defect)																		
		<table border="1"> <thead> <tr> <th>Length</th> <th>Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td>/</td> <td><math>W \leq 0.03</math></td> <td>Ignore</td> </tr> <tr> <td><math>L \leq 2.5</math></td> <td><math>0.03 &lt; W \leq 0.05</math></td> <td>3</td> </tr> <tr> <td><math>L \leq 2.5</math></td> <td><math>0.05 &lt; W \leq 0.10</math></td> <td>2</td> </tr> <tr> <td>/</td> <td><math>0.1 &lt; W</math></td> <td>0</td> </tr> <tr> <td colspan="2">Total</td> <td>3</td> </tr> </tbody> </table>	Length	Width	Acc. Qty	/	$W \leq 0.03$	Ignore	$L \leq 2.5$	$0.03 < W \leq 0.05$	3	$L \leq 2.5$	$0.05 < W \leq 0.10$	2	/	$0.1 < W$	0	Total	
Length	Width	Acc. Qty																	
/	$W \leq 0.03$	Ignore																	
$L \leq 2.5$	$0.03 < W \leq 0.05$	3																	
$L \leq 2.5$	$0.05 < W \leq 0.10$	2																	
/	$0.1 < W$	0																	
Total		3																	
		<p>Distance between 2 defects should more than 3mm apart. Scratches not viewable through the back of the display are acceptable.</p>																	
04	Glass Crack (Minor defect)	<p>Crack is potential to enlarge, any type is not allowed.</p>																	



<p>05</p>	<p>Glass Chipping Pad Area: (Minor defect)</p> 	<table border="1"> <thead> <tr> <th>Length and Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>c &gt; 3.0, b &lt; 1.0</math></td> <td>1</td> </tr> <tr> <td><math>c &lt; 3.0, b &lt; 1.0</math></td> <td>3</td> </tr> <tr> <td colspan="2"><math>a &lt; \text{Glass Thickness}</math></td> </tr> </tbody> </table>	Length and Width	Acc. Qty	$c > 3.0, b < 1.0$	1	$c < 3.0, b < 1.0$	3	$a < \text{Glass Thickness}$			
Length and Width	Acc. Qty											
$c > 3.0, b < 1.0$	1											
$c < 3.0, b < 1.0$	3											
$a < \text{Glass Thickness}$												
<p>06</p>	<p>Glass Chipping Rear of Pad Area: (Minor defect)</p> 	<table border="1"> <thead> <tr> <th>Length and Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>c &gt; 3.0, b &lt; 1.0</math></td> <td>1</td> </tr> <tr> <td><math>c &lt; 3.0, b &lt; 1.0</math></td> <td>2</td> </tr> <tr> <td><math>c &lt; 3.0, b &lt; 0.5</math></td> <td>4</td> </tr> <tr> <td colspan="2"><math>a &lt; \text{Glass Thickness}</math></td> </tr> </tbody> </table>	Length and Width	Acc. Qty	$c > 3.0, b < 1.0$	1	$c < 3.0, b < 1.0$	2	$c < 3.0, b < 0.5$	4	$a < \text{Glass Thickness}$	
Length and Width	Acc. Qty											
$c > 3.0, b < 1.0$	1											
$c < 3.0, b < 1.0$	2											
$c < 3.0, b < 0.5$	4											
$a < \text{Glass Thickness}$												
<p>07</p>	<p>Glass Chipping Except Pad Area: (Minor defect)</p> 	<table border="1"> <thead> <tr> <th>Length and Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>c &gt; 3.0, b &lt; 1.0</math></td> <td>1</td> </tr> <tr> <td><math>c &lt; 3.0, b &lt; 1.0</math></td> <td>2</td> </tr> <tr> <td><math>c &lt; 3.0, b &lt; 0.5</math></td> <td>4</td> </tr> <tr> <td colspan="2"><math>a &lt; \text{Glass Thickness}</math></td> </tr> </tbody> </table>	Length and Width	Acc. Qty	$c > 3.0, b < 1.0$	1	$c < 3.0, b < 1.0$	2	$c < 3.0, b < 0.5$	4	$a < \text{Glass Thickness}$	
Length and Width	Acc. Qty											
$c > 3.0, b < 1.0$	1											
$c < 3.0, b < 1.0$	2											
$c < 3.0, b < 0.5$	4											
$a < \text{Glass Thickness}$												
<p>08</p>	<p>Glass Corner Chipping: (Minor defect)</p> 	<table border="1"> <thead> <tr> <th>Length and Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>c &lt; 3.0, b &lt; 3.0</math></td> <td>Ignore</td> </tr> <tr> <td colspan="2"><math>a &lt; \text{Glass Thickness}</math></td> </tr> </tbody> </table>	Length and Width	Acc. Qty	$c < 3.0, b < 3.0$	Ignore	$a < \text{Glass Thickness}$					
Length and Width	Acc. Qty											
$c < 3.0, b < 3.0$	Ignore											
$a < \text{Glass Thickness}$												

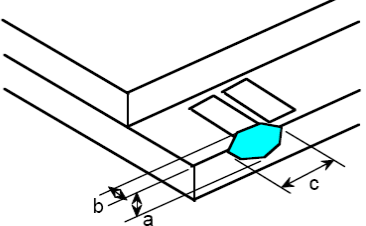
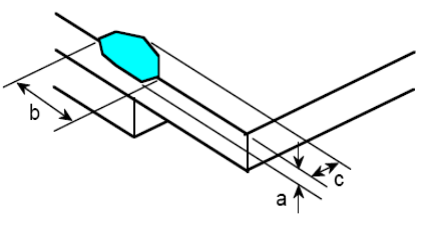
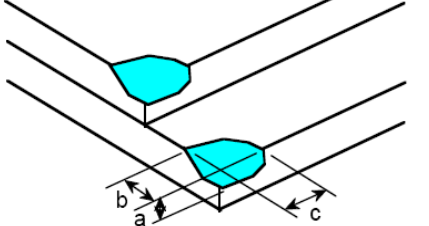
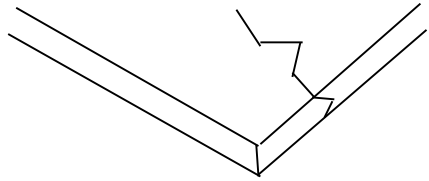
<p>09</p>	<p>Glass Burr: (Minor defect)</p> 	<table border="1" data-bbox="869 264 1340 353"> <thead> <tr> <th>Length</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>F &lt; 1.0</math></td> <td>Ignore</td> </tr> </tbody> </table> <p>Glass burr don't affect assemble and module dimension.</p>	Length	Acc. Qty	$F < 1.0$	Ignore						
Length	Acc. Qty											
$F < 1.0$	Ignore											
<p>10</p>	<p>FPC Defect: (Minor defect)</p> 	<p>10.1 Dent, pinhole width <math>a &lt; w/3</math>. (w: circuitry width.)</p> <p>10.2 Open circuit is unacceptable.</p> <p>10.3 No oxidation, contamination and distortion.</p>										
<p>11</p>	<p>Bubble on Polarizer (Minor defect)</p>	<table border="1" data-bbox="742 1299 1212 1512"> <thead> <tr> <th>Diameter</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>\varphi \leq 0.20</math></td> <td>Ignore</td> </tr> <tr> <td><math>0.20 &lt; \varphi \leq 0.30</math></td> <td>4</td> </tr> <tr> <td><math>0.30 &lt; \varphi \leq 0.50</math></td> <td>1</td> </tr> <tr> <td><math>0.50 &lt; \varphi</math></td> <td>None</td> </tr> </tbody> </table>	Diameter	Acc. Qty	$\varphi \leq 0.20$	Ignore	$0.20 < \varphi \leq 0.30$	4	$0.30 < \varphi \leq 0.50$	1	$0.50 < \varphi$	None
Diameter	Acc. Qty											
$\varphi \leq 0.20$	Ignore											
$0.20 < \varphi \leq 0.30$	4											
$0.30 < \varphi \leq 0.50$	1											
$0.50 < \varphi$	None											
<p>12</p>	<p>Dent on Polarizer (Minor defect)</p>	<table border="1" data-bbox="742 1563 1212 1776"> <thead> <tr> <th>Diameter</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>\varphi \leq 0.20</math></td> <td>Ignore</td> </tr> <tr> <td><math>0.20 &lt; \varphi \leq 0.30</math></td> <td>4</td> </tr> <tr> <td><math>0.30 &lt; \varphi \leq 0.50</math></td> <td>1</td> </tr> <tr> <td><math>0.50 &lt; \varphi</math></td> <td>None</td> </tr> </tbody> </table>	Diameter	Acc. Qty	$\varphi \leq 0.20$	Ignore	$0.20 < \varphi \leq 0.30$	4	$0.30 < \varphi \leq 0.50$	1	$0.50 < \varphi$	None
Diameter	Acc. Qty											
$\varphi \leq 0.20$	Ignore											
$0.20 < \varphi \leq 0.30$	4											
$0.30 < \varphi \leq 0.50$	1											
$0.50 < \varphi$	None											
<p>13</p>	<p>Bezel</p>	<p>13.1 No rust, distortion on the Bezel.</p> <p>13.2 No visible fingerprints, stains or other contamination.</p>										



14	Touch Panel	<p>D: Diameter W: width L: length</p> <p>14.1 Spot: <math>D &lt; 0.25</math> is acceptable  <math>0.25 \leq D \leq 0.4</math></p> <p>2dots are acceptable and the distance between defects should more than 10 mm.</p> <p><math>D &gt; 0.4</math> is unacceptable</p> <p>14.2 Dent: <math>D &gt; 0.40</math> is unacceptable</p> <p>14.3 Scratch: <math>W \leq 0.03</math>, <math>L \leq 10</math> is acceptable,  <math>0.03 &lt; W \leq 0.10</math>, <math>L \leq 10</math> is acceptable</p> <p>Distance between 2 defects should more than 10 mm.  <math>W &gt; 0.10</math> is unacceptable.</p>
15	LCD Ripple	<p>Touch the touch panel, cannot see the LCD ripple.</p> <p>Pen: R 0.8mm silicon rubber.</p> <p>Operation Force:120g</p>
16	PCB	<p>16.1 No distortion or contamination on PCB terminals.</p> <p>16.2 All components on PCB must same as documented on the BOM/component layout.</p> <p>16.3 Follow IPC-A-600F.</p>
17	Soldering	<p>Follow IPC-A-610C standard</p>
18	Electrical Defect (Major defect)	<p>The below defects must be rejected.</p> <p>18.1 Missing vertical / horizontal segment,</p> <p>18.2 Abnormal Display.</p> <p>18.3 No function or no display.</p> <p>18.4 Current exceeds product specifications.</p> <p>18.5 LCD viewing angle defect.</p> <p>18.6 No Backlight.</p> <p>18.7 Dark Backlight.</p> <p>18.8 Touch Panel no function.</p>

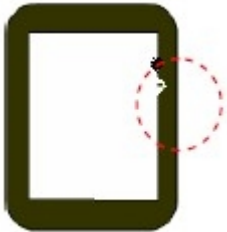
Remark: LCD Panel Broken shall be rejected. Defect out of LCD viewing area is acceptable.

Inspection Specification for the Capacitive Touch Panel

01	<p>Chipping Pad Area(Not include the cover lens):                  (Minor defect)</p>	<p>The chip is seriously influence the product's function, any type is not allowed.</p>
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<p>02</p>	<p>Chipping Except Pad Area(Not include the cover lens): (Minor defect)</p> 	<table border="1"> <thead> <tr> <th>Length and Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>c &lt; 1.5, b &lt; 1</math></td> <td><math>N \leq 5</math></td> </tr> <tr> <td colspan="2"><math>a &lt; 1/2</math> Glass Thickness</td> </tr> </tbody> </table>	Length and Width	Acc. Qty	$c < 1.5, b < 1$	$N \leq 5$	$a < 1/2$ Glass Thickness	
Length and Width	Acc. Qty							
$c < 1.5, b < 1$	$N \leq 5$							
$a < 1/2$ Glass Thickness								
<p>03</p>	<p>Corner Chipping(Not include the cover lens): (Minor defect)</p> 	<table border="1"> <thead> <tr> <th>Length and Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>c &lt; 1.5, b &lt; 0.5</math></td> <td>Ignore</td> </tr> <tr> <td colspan="2"><math>a &lt; 1/2</math> Glass Thickness</td> </tr> </tbody> </table>	Length and Width	Acc. Qty	$c < 1.5, b < 0.5$	Ignore	$a < 1/2$ Glass Thickness	
Length and Width	Acc. Qty							
$c < 1.5, b < 0.5$	Ignore							
$a < 1/2$ Glass Thickness								
<p>04</p>	<p>Crack: (Minor defect)</p>	 <p>Crack is potential to enlarge, any type is not allowed.</p>						

05	Cover lens must be without any chips, cracks or other damage when viewed from the front.																				
06	<p>Same/Different color spot</p>  <p>D: Diameter W: width L: length</p> <table border="1" data-bbox="892 445 1343 580"> <thead> <tr> <th>Diameter</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>D &lt; 0.20</math></td> <td>Ignore</td> </tr> </tbody> </table> <p>Active Area:</p> <table border="1" data-bbox="892 627 1343 846"> <thead> <tr> <th>Diameter</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>0.20 &lt; D \leq 0.30</math></td> <td>2</td> </tr> <tr> <td><math>0.30 &lt; D \leq 0.50</math></td> <td>1</td> </tr> <tr> <td><math>D &gt; 0.5</math></td> <td>NG</td> </tr> </tbody> </table> <p>Viewing Area :</p> <table border="1" data-bbox="892 896 1343 1131"> <thead> <tr> <th>Diameter</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td><math>D &lt; 0.20</math></td> <td>Ignore</td> </tr> <tr> <td><math>0.20 &lt; D \leq 0.5</math></td> <td>3</td> </tr> <tr> <td><math>D &gt; 0.5</math></td> <td>NG</td> </tr> </tbody> </table> <p>Distance between 2 defects should more than 15mm apart.</p>	Diameter	Acc. Qty	$D < 0.20$	Ignore	Diameter	Acc. Qty	$0.20 < D \leq 0.30$	2	$0.30 < D \leq 0.50$	1	$D > 0.5$	NG	Diameter	Acc. Qty	$D < 0.20$	Ignore	$0.20 < D \leq 0.5$	3	$D > 0.5$	NG
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$D > 0.5$	NG																				
07	<p>Cover lens line Scratch</p>  <table border="1" data-bbox="794 1350 1422 1657"> <thead> <tr> <th>Length</th> <th>Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td>/</td> <td><math>W \leq 0.08\text{mm}</math></td> <td>Ignore</td> </tr> <tr> <td><math>L \leq 5</math></td> <td><math>0.08 &lt; W \leq 0.15</math></td> <td>2</td> </tr> <tr> <td><math>L \leq 3</math></td> <td><math>0.15 &lt; W \leq 0.20</math></td> <td>1</td> </tr> <tr> <td>-</td> <td><math>W &gt; 0.2</math></td> <td>NG</td> </tr> <tr> <td><math>L &gt; 5</math></td> <td>-</td> <td>NG</td> </tr> </tbody> </table> <p>Distance between 2 defects should more than 15mm apart.</p>	Length	Width	Acc. Qty	/	$W \leq 0.08\text{mm}$	Ignore	$L \leq 5$	$0.08 < W \leq 0.15$	2	$L \leq 3$	$0.15 < W \leq 0.20$	1	-	$W > 0.2$	NG	$L > 5$	-	NG		
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-	$W > 0.2$	NG																			
$L > 5$	-	NG																			

08	Printing sawtooth 														
	<table border="1"> <thead> <tr> <th style="width: 25%;">Length</th> <th style="width: 40%;">Width</th> <th style="width: 15%;">Acc. Qty</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">/</td> <td style="text-align: center;"><math>W \leq 0.2\text{mm}</math></td> <td style="text-align: center;">2</td> </tr> <tr> <td style="text-align: center;"><math>L \leq 2</math></td> <td style="text-align: center;"><math>0.2 &lt; W \leq 0.3</math></td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;"><math>L \leq 2</math></td> <td style="text-align: center;"><math>W &gt; 0.3</math></td> <td style="text-align: center;">NG</td> </tr> </tbody> </table>	Length	Width	Acc. Qty	/	$W \leq 0.2\text{mm}$	2	$L \leq 2$	$0.2 < W \leq 0.3$	1	$L \leq 2$	$W > 0.3$	NG		
	Length	Width	Acc. Qty												
	/	$W \leq 0.2\text{mm}$	2												
$L \leq 2$	$0.2 < W \leq 0.3$	1													
$L \leq 2$	$W > 0.3$	NG													

**12.7. Classification of Defects**

12.7.1 Visual defects (Except no / wrong label) are treated as minor defect and electrical defect is major.

12.7.2 Two minor defects are equal to one major in lot sampling inspection.

**12.8. Identification/marketing criteria**

Any unit with illegible / wrong /double or no marking/ label shall be rejected.

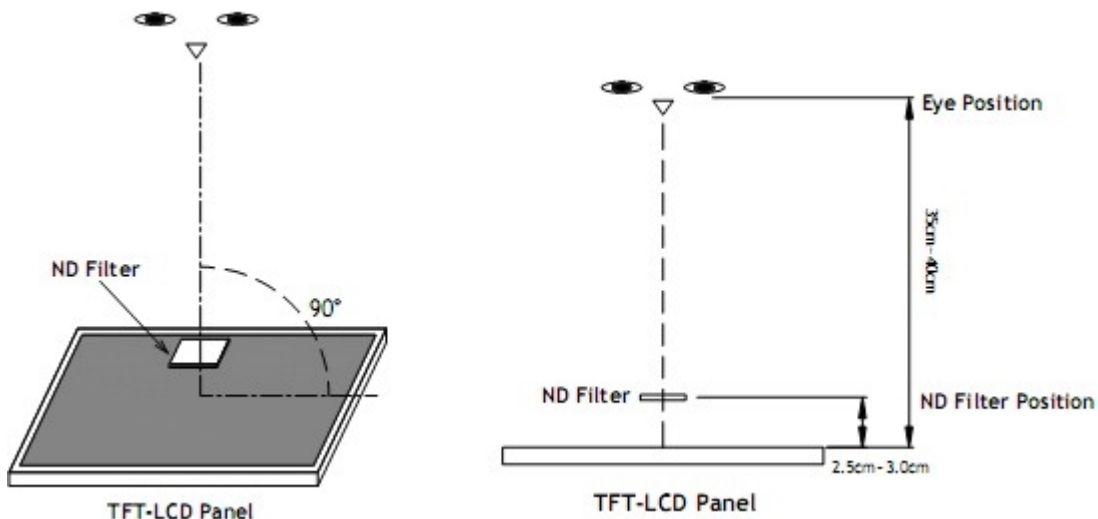
**12.9. Packaging**

12.9.1 There should be no damage of the outside carton box, each packaging box should have one identical label.

12.9.2 Modules inside package box should have compliant mark.

12.9.3 All direct package materials shall offer ESD protection

**Note1:** Bright dot is defined as the defective area of the dot is larger than 50% of one sub-pixel area.



Bright dot: The bright dot size defect at black display pattern. It can be recognized by 2% transparency of filter when the distance between eyes and panel is  $350\text{mm} \pm 50\text{mm}$ .

Dark dot: Cyan, Magenta or Yellow dot size defect at white display pattern. It can be recognized by 5% transparency of filter when the distance between eyes and panel is  $350\text{mm} \pm 50\text{mm}$ .

**Note2:** Mura on display which appears darker / brighter against background brightness on parts of display area.

**13. Reliability Specification**

No	Item	Condition	Quantity	Criteria
1	High Temperature Operating	+70°C, 96Hrs	2	GB/T2423.2-2008
2	Low Temperature Operating	-20°C, 96Hrs	2	GB/T2423.1-2008
3	High Humidity	+50°C, 90%RH, 96Hrs	2	GB/T2423.3-2006
4	High Temperature Storage	+80°C, 96Hrs	2	GB/T2423.2-2008
5	Low Temperature Storage	-30°C, 96Hrs	2	GB/T2423.1-2008
6	Thermal Cycling Test	-20°C, 60min~+70°C, 60min, 20 cycles.	2	GB/T2423.22-2012
7	Packing vibration	Frequency range:10Hz~50Hz Acceleration of gravity:5G X, Y, Z 30 min for each direction.	2	GB/T5170.14-2009
8	Electrical Static Discharge	Air: ±8KV 150pF/330Ω 5 times	2	GB/T17626.2-2006
		Contact: ±4KV 150pF/330Ω 5 times		
9	Drop Test (Packaged)	Height:80 cm,1 corner, 3 edges, 6 surfaces.	2	GB/T2423.8-1995

Note1. No deflection cosmetic and operational function allowable.

Note2. Total current Consumption should be below double of initial value.

**14. Precautions and Warranty**

**14.1 Safety**

- 14.1.1. The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.
- 14.1.2. Since the liquid crystal cells are made of glass, do not apply strong impact on them. Handle with care.

**14.2. Handling**

- 14.2.1. Reverse and use within ratings in order to keep performance and prevent damage.
- 14.2.2. Do not wipe the polarizer with dry cloth, as it might cause scratch. If the surface of the LCD needs to be cleaned, wipe it swiftly with cotton or other soft cloth soaked with petroleum IPA, do not use other chemicals.

**14.3. Storage**

- 14.3.1 Do not store the LCD module beyond the specified temperature ranges.

**14.4. Metal Pin (Apply to Products with Metal Pins)**

14.4.1. Pins of LCD and Backlight

- 14.4.1.1. Solder tip can touch and press on the tip of Pin LEAD during the soldering

14.4.1.2. Recommended Soldering Conditions

Solder Type: Sn96.3~94-Ag3.3~4.3-Cu0.4~1.1

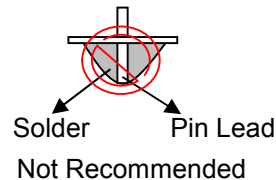
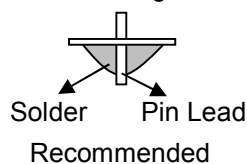
Maximum Solder Temperature: 370℃

Maximum Solder Time: 3s at the maximum temperature

Recommended Soldering Temp: 350±20℃

Typical Soldering Time: ≤3s

14.4.1.3. Solder Wetting



14.4.2. Pins of EL

- 14.4.2.1. Solder tip can touch and press on the tip of EL leads during soldering.

- 14.4.2.2. No Solder Paste on the soldering pad on the motherboard is recommended.

14.4.2.3. Recommended Soldering Conditions

Solder type: Nippon Alimit Leadfree SR-34, size 0.5mm

Recommended Solder Temperature: 270~290℃

Typical Soldering Time: ≤2s

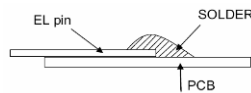
Minimum solder distance from EL lamp (body):2.0mm

- 14.4.2.4. No horizontal press on the EL leads during soldering.

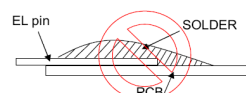
- 14.4.2.5. 180° bend EL leads three times is not allowed.



14.4.2.6. Solder Wetting

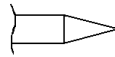


Recommended

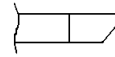


Not Recommended

14.4.2.7. The type of the solder iron:

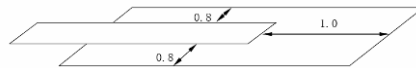


Recommended



Not Recommended

14.4.2.8. Solder Pad



**14.5. Operation**

- 14.5.1. Do not drive LCD with DC voltage
- 14.5.2. Response time will increase below lower temperature
- 14.5.3. Display may change color with different temperature
- 14.5.4. Mechanical disturbance during operation, such as pressing on the display area, may cause the segments to appear “fractured”.

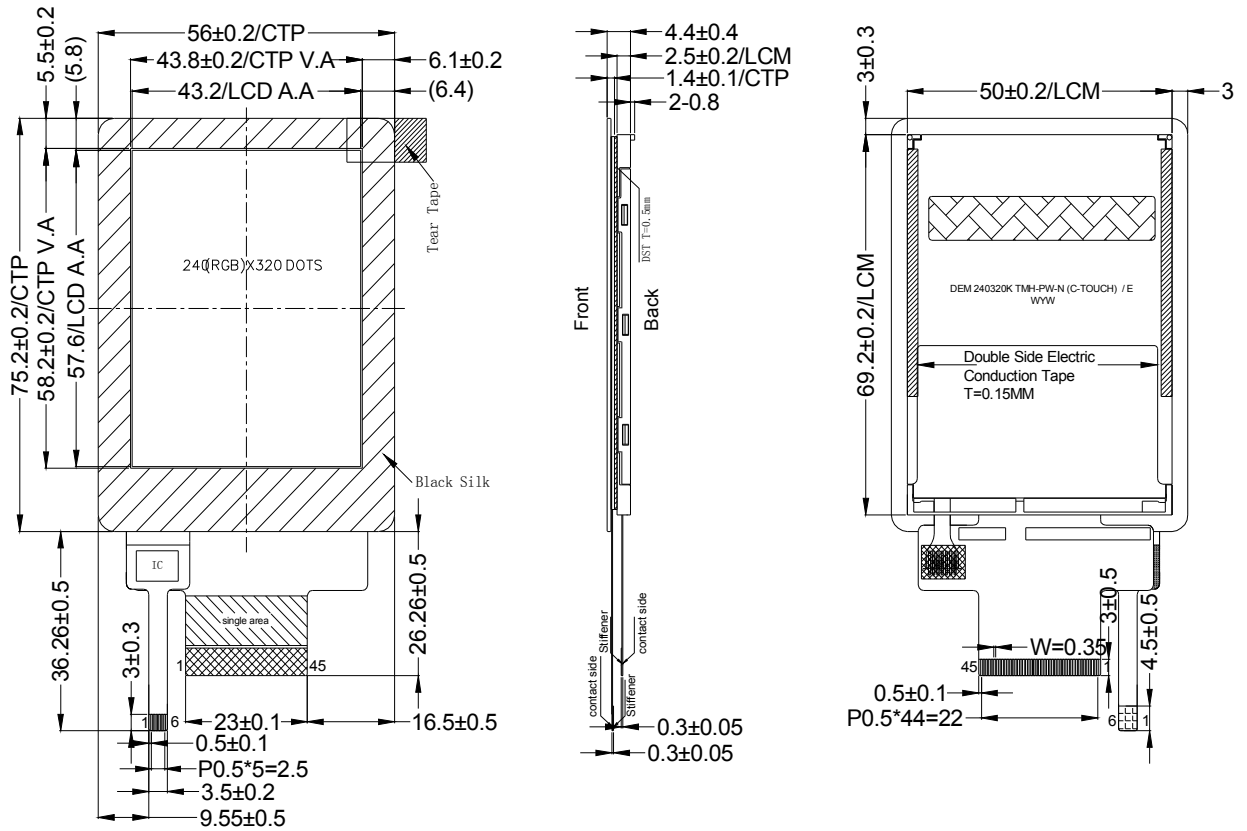
**14.6. Static Electricity**

- 14.6.1. CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro-static charge, by ground human body, etc.
- 14.6.2. The normal static prevention measures should be observed for work clothes and benches.
- 14.6.3. The module should be kept into anti-static bags or other containers resistant to static for storage.

**14.7. Limited Warranty**

- 14.7.1. Our warranty liability is limited to repair and/or replacement. We will not be responsible for any consequential loss.
- 14.7.2. If possible, we suggest customer to use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used.
- 14.7.3. After the product shipped, any product quality issues must be feedback within three months, otherwise, we will not be responsible for the subsequent or consequential events.

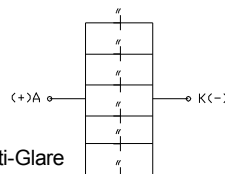
15. Outline Drawing



NOTES:

1. Display Size: 2.8" TFT
2. Viewing direction: 6:00
3. Grey Scale Inversion Direction: 12:00
4. Display Mode: Transmissive / Normal White / Anti-Glare
5. Operation Temperature: -20°C to +70°C
6. Storage Temperature: -30°C to +80°C
7. Driver IC: ILI9341V (Ilitek)
8. Power Supply Voltage: 2.8V (typ.)
9. Backlight: White(6xLED) / 3.2V/120mA (typ.)
10. Luminance: 380cd/m2 (typ.)
11. LED Lifetime: 20000h (typ.)

\* Unspecification Tolerances are ±0.2mm



Technical Parameters:

1. Cover Glass+LOCA+ITO GLASS+FPC
- ITO Glass: T=0.55mm
- Cover Glas: 0.7mm
- Lead Line: FPC
- IC Model: FT5336 (Focaltech)
2. Operation Voltage: 2.8V-3.3V
3. Transmittance: =85%
4. Surface Hardness: =6H
5. Operation Environment: -20°C to +70°C
6. Storage Environment: -30°C to +80°C

CTP

PIN	SYMBOL
1	GND
2	SCL
3	SDA
4	INT
5	RESET
6	VCC

PIN	ASSIGNMENT
1	EXTC
2	iovcc(1.8/2.8v)
3	vcc(2.8v)
4	/CS
5	D/C(SCL)
6	/WR
7	/RD
8	/RESET
9	DB0
10	DB1
11	DB2
12	DB3
13	DB4
14	DB5
15	DB6
16	DB7
17	DB8
18	DB9
19	DB10
20	DB11
21	DB12
22	DB13
23	DB14
24	DB15
25	DB16
26	DB17
27	SDA
28	SDO
29	TE
30	DOTCLK
31	VSYNC
32	HSYNC
33	ENABLE
34	IM0
35	IM1
36	IM2
37	IM3
38	NC(YD)
39	NC(XR)
40	NC(YU)
41	NC(XL)
42	LED_A
43	LED_K
44	GND
45	GND