Displav Elektronik GmbH

DATA SHEET

LCD MODULE

DEM 128128D FGH-PW

Product Specification ***Version: 3***

17.01.2019

GENERAL SPECIFICATION

MODULE NO. :

DEM 128128D FGH-PW

CUSTOMER P/N**:**

Version No.	Change Description	Date
0	Original Version	18.12.2009
1	Update Functions & Features, Dimensional Outline and Electro-Optical Characteristics	28.03.2014
1.1.0	Change Production Line	12.07.2018
1.1.1	Correct the P/N in the drawing ;Add the A/K in the drawing;Update the LED circuit in the BL drawing.	12.12.2018
2	Change the Vop to 11.8V from 12.5V;Update the LCD drawing(IC layout) on page 19	26.12.2018
3	Correct the Vop to 12.5V	17.01.2019

PREPARED BY: PS **DATE:** 17.01.2019

APPROVED BY: MHI **DATE:** 17.01.2019

CONTENTS

1. FUNCTIONS & FEATURES

- DEM 128128D FGH-PW Series LCD Type :

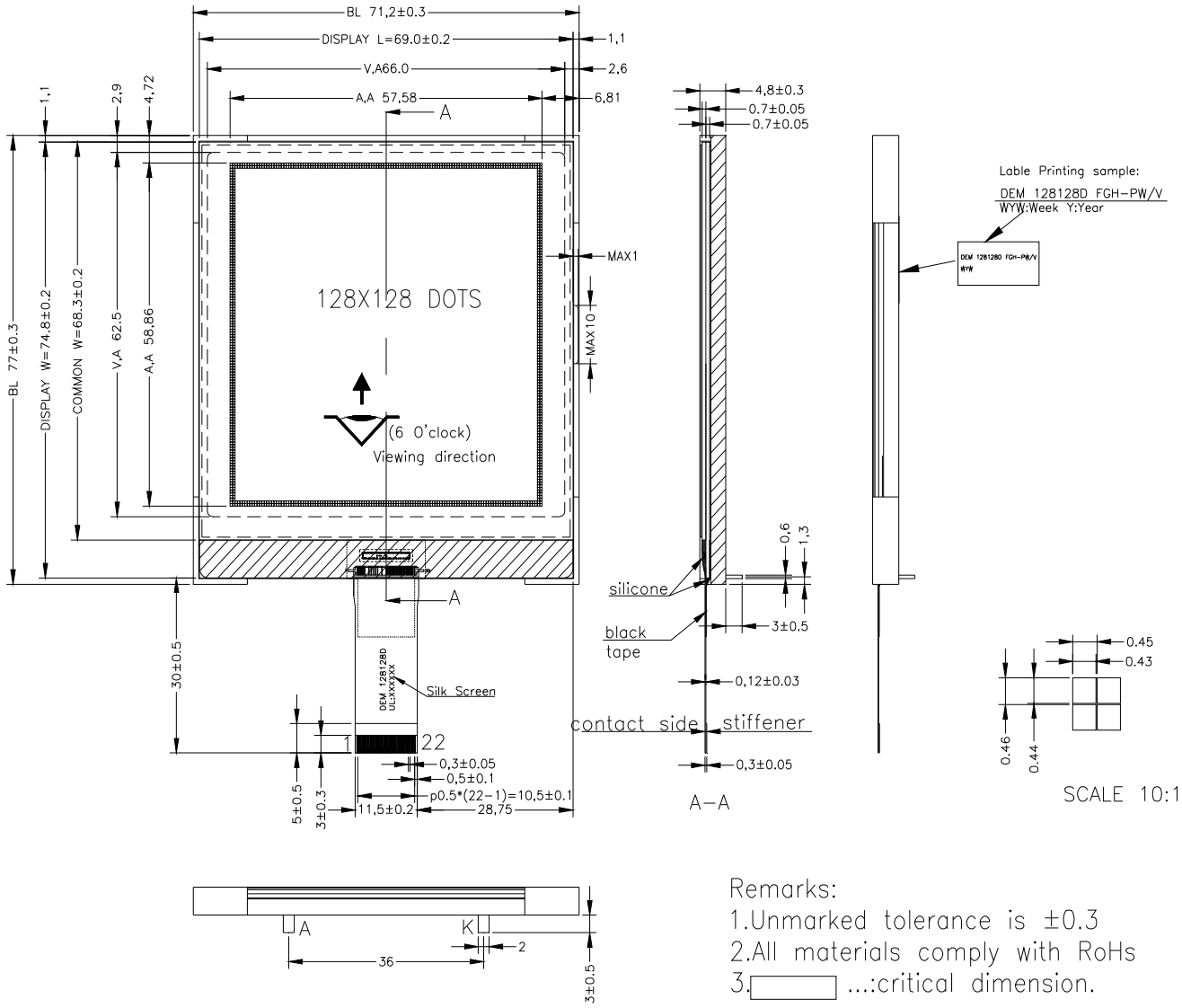
Module	LCD Type	Remark
DEM 128128D FGH-PW	FSTN Transflective Positive Mode	-

- Format : 128 x 128 Dots
- Driving Scheme : 1/128 Duty, 1/11 Bias
- Viewing Direction : 6 0'clock
- Power Supply Voltage(V_{DD}) : 3.0V (typ.)
- LCD driving voltage(V_{LCD}) : 12.5V (typ.)
- Operation Temperature : -20 to + 70 °C
- Storage Temperature : -30 to + 80 °C
- Backlight : LED, Lightguide, White
- RoHS Compliant

2. MECHANICAL SPECIFICATIONS

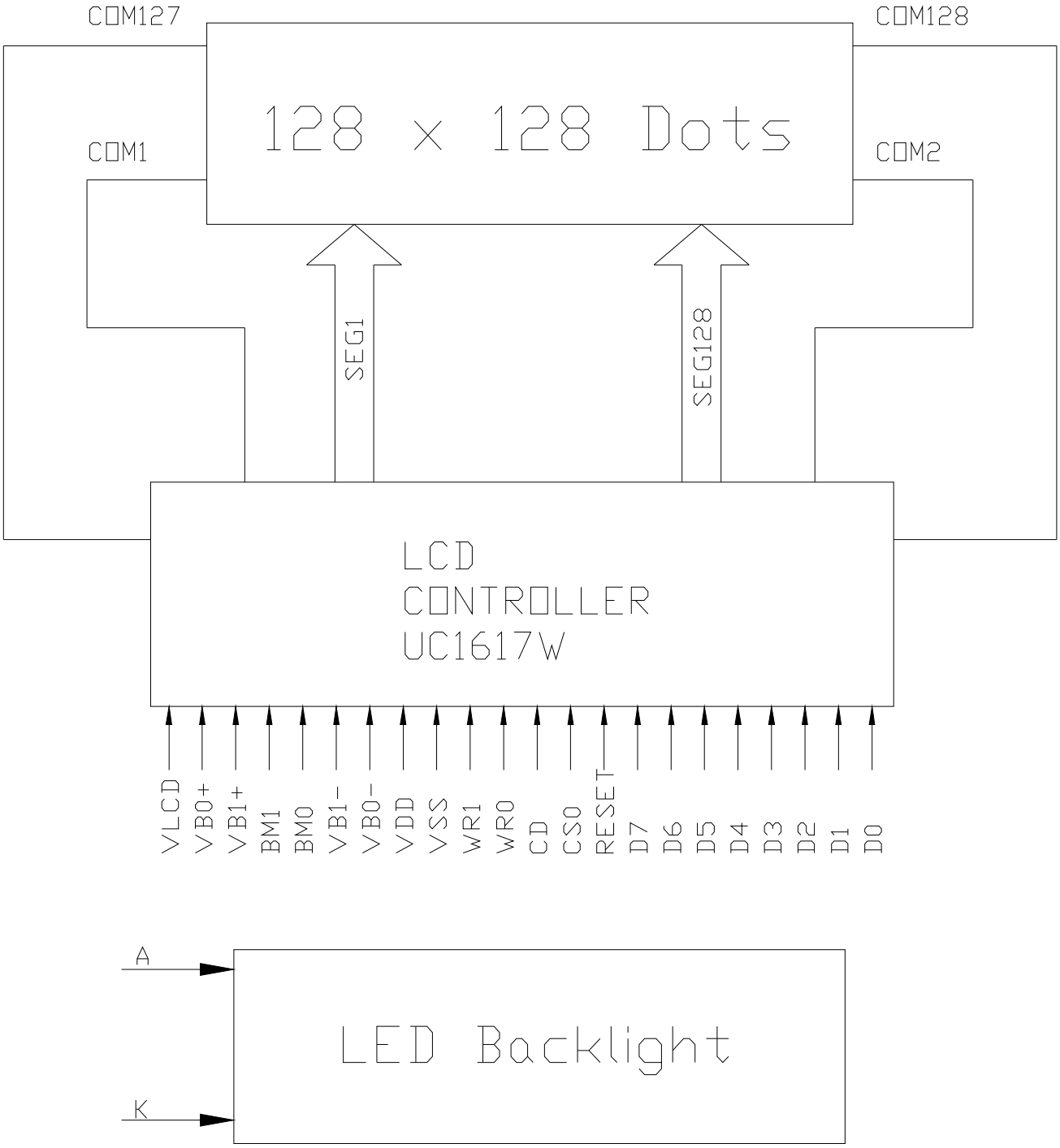
- Module Size : 71.20 x 77.00 x 4.80 mm (without FPC length)
- Viewing Area : 66.00 x 62.50 mm
- Active Area : 57.58 x 58.86 mm
- Dot Pitch : 0.45 x 0.46 mm
- Dot Size : 0.43 x 0.44 mm
- Dot Gap : 0.02 mm

3. EXTERNAL DIMENSIONS



Remarks:
1.Unmarked tolerance is ±0.3
2.All materials comply with RoHs
3. ☐ ...:critical dimension.

4. BLOCK DIAGRAM

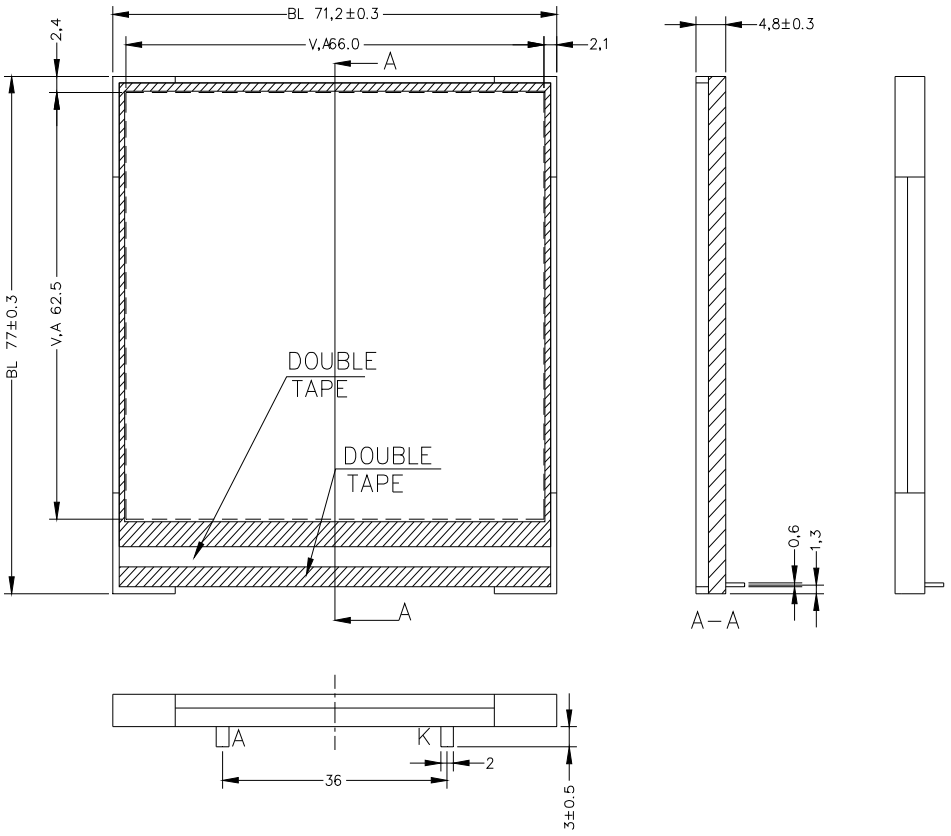


5. PIN ASSIGNMENT

<table>
<tr><th>PIN No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>VLCD</td><td>Main LCD Power Supply</td></tr>
<tr><td>2</td><td>VB0+</td><td rowspan="2">LCD Bias Voltages.</td></tr>
<tr><td>3</td><td>VB1+</td></tr>
<tr><td>4</td><td>BM1</td><td rowspan="2">Bus mode The interfece bus mode is determined by BM[1:0] and D[7:6]by the following relationship:
<table>
<tr><th>BM[1:0]</th><th>D[7:6]</th><th>Mode</th></tr>
<tr><td>11</td><td>Data</td><td>6800/8-bit</td></tr>
<tr><td>10</td><td>Data</td><td>8080/8-bit</td></tr>
<tr><td>01</td><td>11</td><td>2-wire I^{2}C</td></tr>
<tr><td>00</td><td>10</td><td>4-wire SPI w/8-bit token (S8:conventional)</td></tr>
<tr><td>00</td><td>11</td><td>3-wire SPI w/8-bit token (S8uc: Ultra-Compact)</td></tr>
</table></td></tr>
<tr><td>5</td><td>BM0</td></tr>
<tr><td>6</td><td>VB1-</td><td rowspan="2">LCD Bias Voltages.</td></tr>
<tr><td>7</td><td>VB0-</td></tr>
<tr><td>8</td><td>VDD</td><td>Power supply (+3.0V)</td></tr>
<tr><td>9</td><td>VSS</td><td>Ground of chip (0V)</td></tr>
<tr><td>10</td><td>WR1</td><td rowspan="2">WR[1:0] controls the read/write operation of the host interface. See section *Host Interface* for more detail.
In parallel mode, WR[1:0] meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to VSS.</td></tr>
<tr><td>11</td><td>WR0</td></tr>
<tr><td>12</td><td>CD</td><td>Select Control data or Display data for read/write operation. In I2C mode, CD pin is not used. Connect CD to VSS when not used.
”L”: Control data ”H”: Display data</td></tr>
<tr><td>13</td><td>CS0</td><td>Chip Select</td></tr>
<tr><td>14</td><td>RESET</td><td>When RST=”L”, all control registers are re-initialized by their default states. Since UC1617 has built-in Power-ON Reset and Software Reset command, RST pin is not required for proper chip operation.
An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to VDD.</td></tr>
<tr><td>15</td><td>D7</td><td rowspan="8">Bi-directional bus for both serial and parallel host interfaces.
In serial modes, connect D[0] to SCK, D[3] to SDA,
<table>
<tr><th></th><th>BM=1x (Parallel)</th><th>BM=01 (I^{2}C)</th><th>BM=00 (S8/S8uc)</th></tr>
<tr><td>D0</td><td>D0</td><td>SCK</td><td>SCK</td></tr>
<tr><td>D1</td><td>D1</td><td>–</td><td>–</td></tr>
<tr><td>D2</td><td>D2</td><td>–</td><td>–</td></tr>
<tr><td>D3</td><td>D3</td><td>SDA</td><td>SDA</td></tr>
<tr><td>D4</td><td>D4</td><td>–</td><td>–</td></tr>
<tr><td>D5</td><td>D5</td><td>–</td><td>–</td></tr>
<tr><td>D6</td><td>D6</td><td>1</td><td>S8/S8uc</td></tr>
<tr><td>D7</td><td>D7</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>16</td><td>D6</td></tr>
<tr><td>17</td><td>D5</td></tr>
<tr><td>18</td><td>D4</td></tr>
<tr><td>19</td><td>D3</td></tr>
<tr><td>20</td><td>D2</td></tr>
<tr><td>21</td><td>D1</td></tr>
<tr><td>22</td><td>D0</td></tr>
<tr><td colspan="3"></td></tr>
<tr><td colspan="2">LED+(A)</td><td>Supply voltage for backlight LED+</td></tr>
<tr><td colspan="2">LED-(K)</td><td>Supply voltage for backlight LED-</td></tr>
</table>

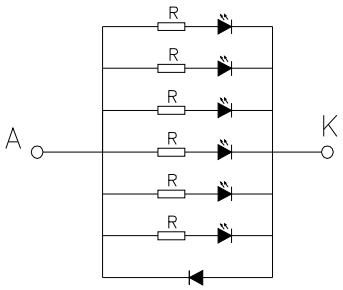
6. BACKLIGHT ELECTRICAL/OPTICAL SPECIFCATIONS

Item	Symbol	min.	typ.	max.	Unit	Condition
Forward Voltagt	Vf	3.3	3.5	3.7	V	If= 60 mA
Power Dissipation	Pd	198	210	222	mW	
Luminous Uniformity	ΔLv	70			%	
Luminance	Lv	350	550		cd/m ^{2}	
Color Coordinate	X	0.260		0.30		T=25 °C
	Y	0.260		0.30		
Lifetime	50000h				Hour	



Circuit Diagram

COLOR: WHITE



Remarks:
1.Unmarked tolerance is ±0.3
2.All materials comply with RoHs
3. [ ]...: critical dimension.

7. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply Voltage	-0.3	+4.0	V
V_{LCD}	LCD Generated Voltage	-0.3	+19.8	V
V_{IN}	Digital Input Signal	-0.4	V_{DD}+ 0.5	V
T_{OPR}	Operating Temperature Range	-20	+70	℃
T_{STR}	Storage Temperature Range	-30	+80	℃

8. ELECTRICAL CHARACTERISTICS

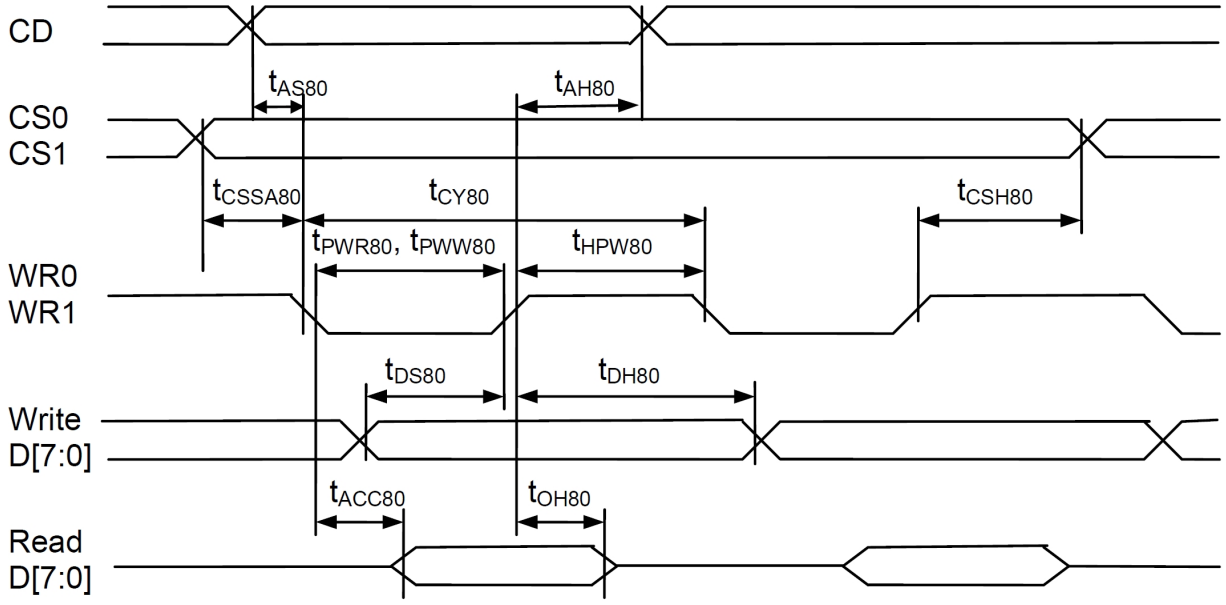
8-1 DC characteristics

Item	Symbol	Min	Typ	Max	Condition	Unit	Remark
Operating Voltage	V_{DD}	2.7	3.0	3.3		V	
LCD Driving Voltage(B00)	V_{LCD}	11.7	12.0	12.3		V	
LCD Driving Voltage(B01)	V_{LCD}	12.2	12.5	12.8			
Operating Current	I_{DD}	---	TBD	---		mA	

8-2 AC characteristics

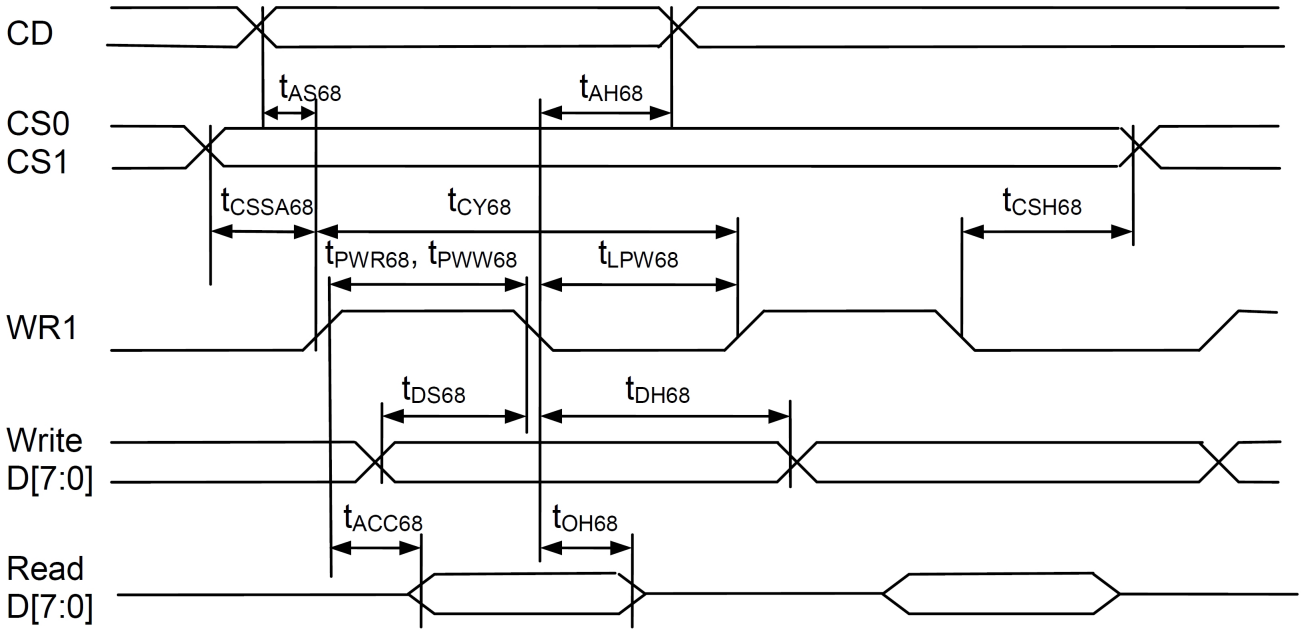
Parallel Bus Timing Characteristics (for 8080 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY80}		System cycle time (read) (write)		170 130	–	nS
t_{PWR80}	WR1	Pulse width (read)		85	–	nS
t_{PWW80}	WR0	Pulse width (write)		65	–	nS
t_{HPW80}	WR0, WR1	High pulse width (read) (write)		85 65	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 0	–	nS
t_{ACC80} t_{OH80}		Read access time Output disable time	C_L = 100pF	– –	65 30	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS



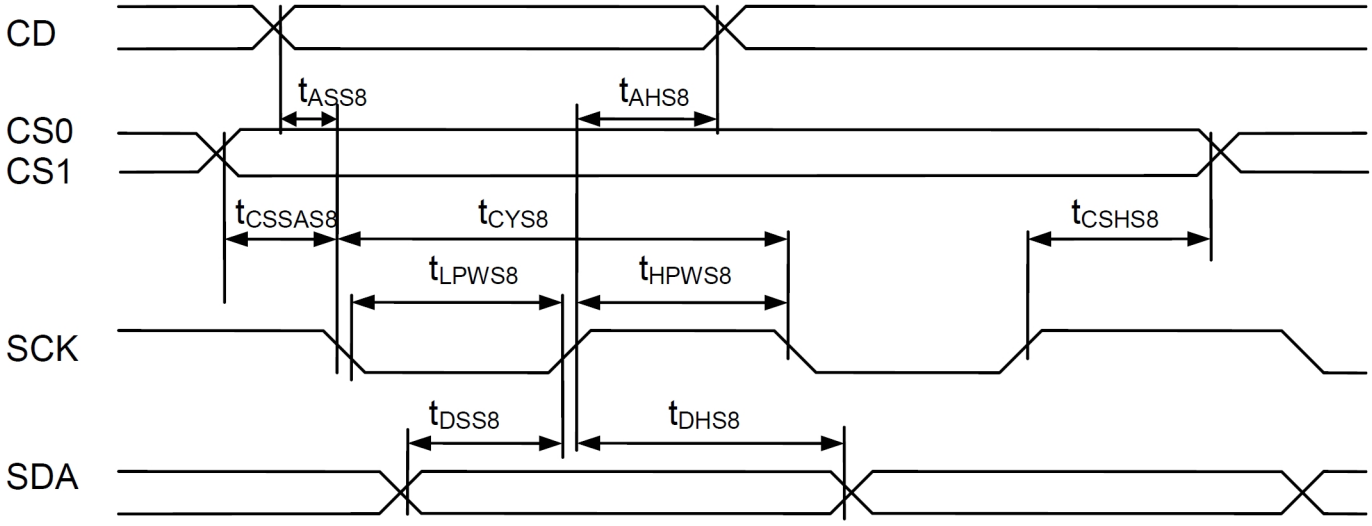
Parallel Bus Timing Characteristics (for 6800 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY68}		System cycle time (read) (write)		170 130	–	nS
t_{PWR68}	WR1	Pulse width (read)		85	–	nS
t_{PWW68}		Pulse width (write)		65	–	nS
t_{LPW68}		Low pulse width (read) (write)		85 65	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 0	–	nS
t_{ACC68} t_{OH68}		Read access time Output disable time	C_L = 100pF	– –	70 30	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS



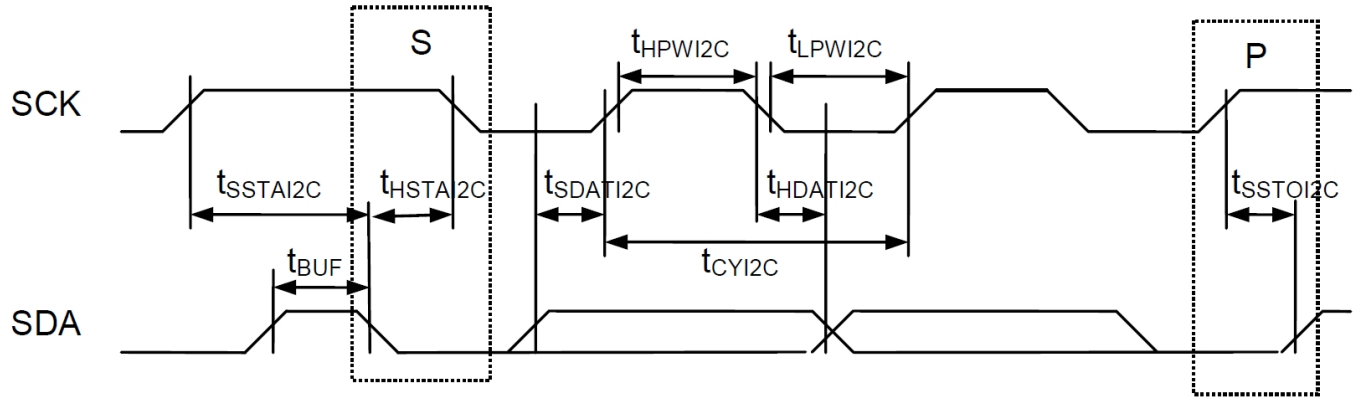
Serial Bus Timing Characteristics (for S8 / S8uc)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		40	–	nS
t_{LPWS8}		Low pulse width		20	–	nS
t_{HPWS8}		High pulse width		20	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data disable time		15 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS



Serial Bus Timing Characteristics (for I2C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYI2C}	SCK	SCK cycle time (read) (write)	tr+tf ⩽ 100nS	580 275	–	nS
t_{LPWI2C}		Low pulse width (read) (write)		290 165	–	nS
t_{HPWI2C}		High pulse width (read) (write)		290 110	–	nS
tr, tf	SCK SDA	Rise time and fall time		–	–	nS
$t_{SSDAI2C}$		Data setup time		28	–	nS
t_{HDAI2C}		Data hold time		11	–	nS
$t_{SSTAI2C}$		START Setup time		28	–	nS
$t_{HSTAI2C}$		START Hold time		28	–	nS
$t_{SSTOI2C}$		STOP setup time		28	–	nS
T_{BUF}		Bus Free time between STOP and START condition		165	–	nS



9. COMMAND TABLE

The following is a list of host commands supported by UC1617

C/D: 0: Control, 1: Data

W/R: 0: Write Cycle, 1: Read Cycle

Useful Data bits

– Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status	0	1	1	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Product Code, PID, MID}	N/A
				Ver		PMO[5:0]							
				Product Code				PID		MID			
4	Set Page_C Address	0	0	0	0	0	#	#	#	#	#	Set CA[4:0]	0H
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b
6	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b
8	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	0	R	R	Set APC[R][7:0], R = 0, 1 or 2	N/A
		0	0	#	#	#	#	#	#	#	#		
9	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0H
	Set Scroll Line MSB	0	0	0	1	0	1	-	#	#	#	Set SL[6:4]	0H
10	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	00H
	Set Row Address MSB	0	0	0	1	1	1	-	#	#	#	Set RA[6:4]	00H
11	Set V_{BIAS} Potentiometer (double-byte command)	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set PM[7:0]	4EH
12	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[9:8]	00b: Disable
13	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14	Set Fixed Lines	0	0	1 #	0 #	0 #	1 #	0 #	0 #	0 #	0 #	Set {FLT, FLB}	0
15	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	00b
16	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
17	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
18	Set Display Enable	0	0	1	0	1	0	1	1	#	#	Set DC[3:2]	10b
19	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	000b
20	Set N-Line Inversion	0	0	1 -	1 -	0 -	0 -	1 #	0 #	0 #	0 #	Set NIV[3:0]	6H
21	Set LCD Gray Shade	0	0	1	1	0	1	0	#	#	#	Set LC[7:5]	001b
22	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
23	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
24	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
25	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 11
26	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	AC[3]=0
27	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	AC[3]=1
28	Set COM End	0 0	0 0	1 -	1 #	1 #	1 #	0 #	0 #	0 #	1 #	Set CEN[6:0]	127
29	Set Partial Display Start	0 0	0 0	1 -	1 #	1 #	1 #	0 #	0 #	1 #	0 #	Set DST[6:0]	0
30	Set Partial Display End	0 0	0 0	1 -	1 #	1 #	1 #	0 #	0 #	1 #	1 #	Set DEN[6:0]	127

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action		Default
31	Set Window Program Starting Page_C Address	0 0	0 0	1 -	1 -	1 -	1 #	0 #	1 #	0 #	0 #	Shared with MTP commands	Set WPC0	0
32	Set Window Programming Starting Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set WPP0	0
33	Set Window Programming Ending Page_C Address	0 0	0 0	1 -	1 -	1 -	1 #	0 #	1 #	1 #	0 #		Set WPC1	31
34	Set Window Programming Ending Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set WPP1	127
35	Enable window program	0	0	1	1	1	1	1	0	0	#	Set AC[4]		0: Disable
36	Set MTP Operation control	0 0	0 0	1 -	0 -	1 #	1 #	1 #	0 #	0 #	0 #	Set MTPC[5:0]		10H
37	Set MTP Write Mask	0 0	0 0	1 #	0 #	1 #	1 #	1 #	0 #	0 #	1 #	Set MTPM[7:0]		0
38	Set V_{MTP1} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with Window Program commands	Set MTP1	N/A
39	Set V_{MTP2} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set MTP2	
40	Set MTP Write Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #		Set MTP3	
41	Set MTP Read Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set MTP4	

Notes:

Any bit patterns other than the commands listed above may result in undefined behavior.

The interpretation of commands (37)~(41) depends on register MTPC[3].

Commands (38)~(41) are shared with commands (31)~(34) and have exactly the same code.

When MTPC[3]=0, commands (38)~(41) are interpreted as Window Programming commands.

When MTPC[3]=1, they are the MTP Control commands.

MTPM and PM are actually the same register. Only one of the commands (37 or 11) is valid at any time, and it is determined by MTPC[3].

After MTP-ERASE or MTP-PROGRAM operation, before resuming normal operation, please always

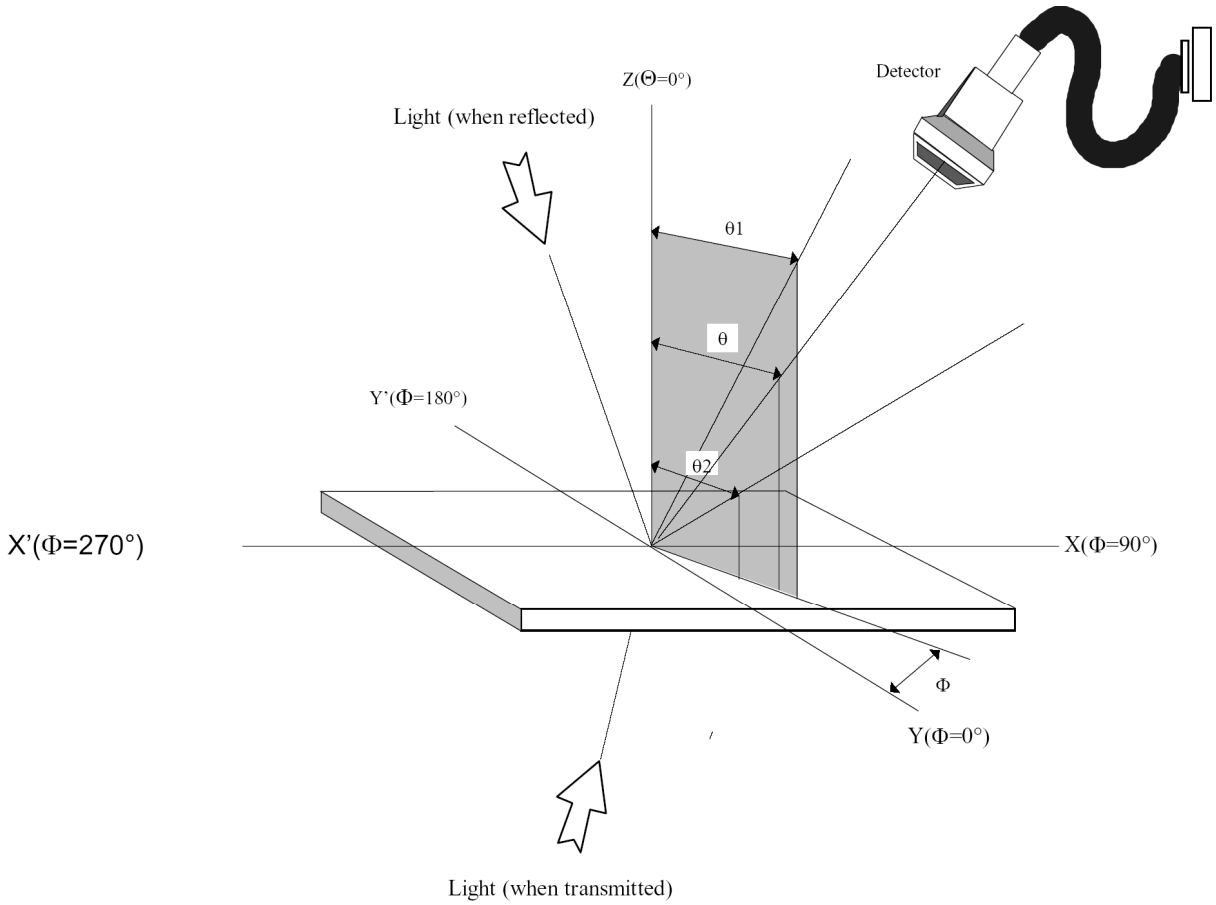
a) Remove TST4 power source,

b) Do a full VDD ON-OFF-ON cycle.

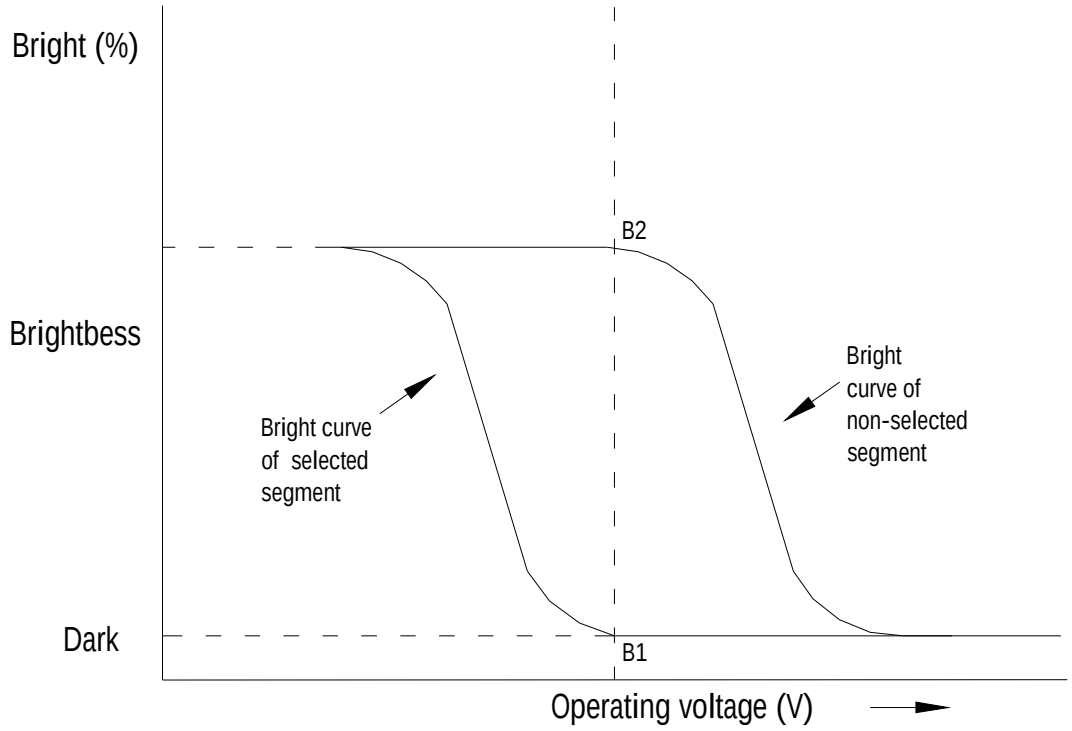
10. ELECTRO-OPTICAL DEFINITION

Optical Characteristics

Item	Symbol	Description	Condition	Min	Typ	Max	Unt
Operating Voltage of LCD	V_{OP}	---	Ta=-20°C	12.6	12.9	13.1	V
		---	Ta=25°C	12.2	12.5	12.8	
		---	Ta=70°C	11.8	12.1	12.4	
Response time	Tr	Rise	25°C	---	250	500	ms
	Tf	Fall	25°C	---	300	600	ms
Contrast	Cr		VDD=3.0V,25°C	2	4	---	
Viewing angle	θ	6 o'clock axis	Cr≥2.0 VDD=3.0V,25°C	---	40	---	Deg
		12 o'clock axis	VDD=3.0V,25°C	---	35	---	Deg
		3 o'clock axis	VDD=3.0V,25°C	---	35	---	Deg
		9 o'clock axis	VDD=3.0V,25°C	---	35	---	Deg

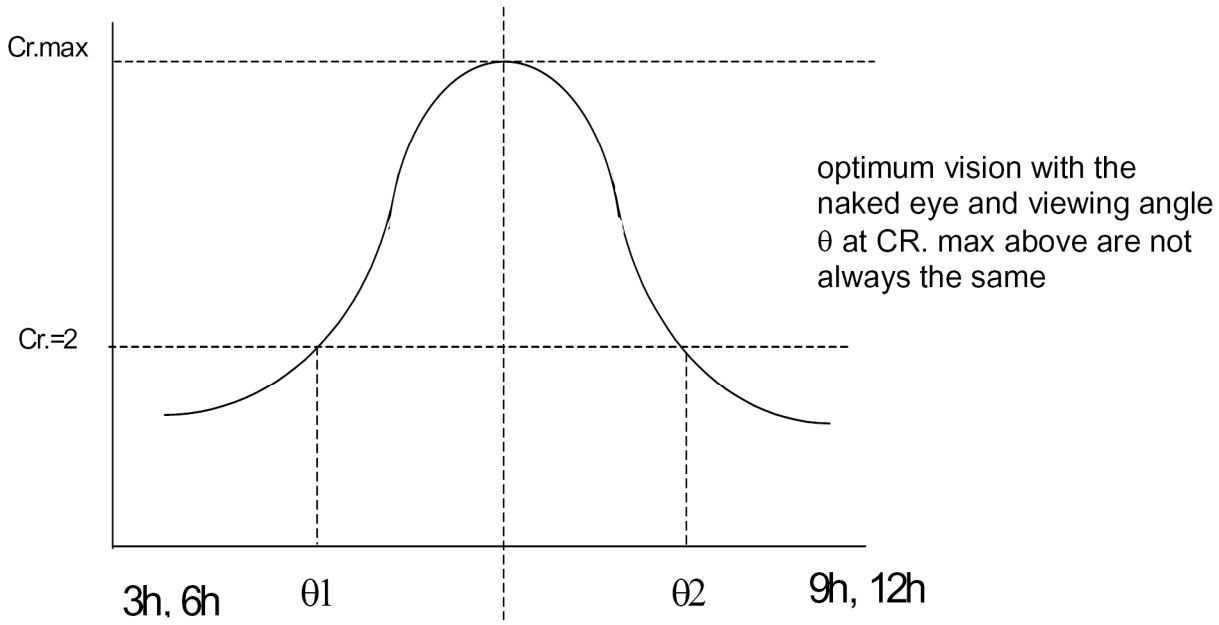


Definition of contrast $Cr. = \frac{B2}{B1} = \frac{\text{Bright curve of not selected segment}}{\text{Bright curve of selected segment}}$

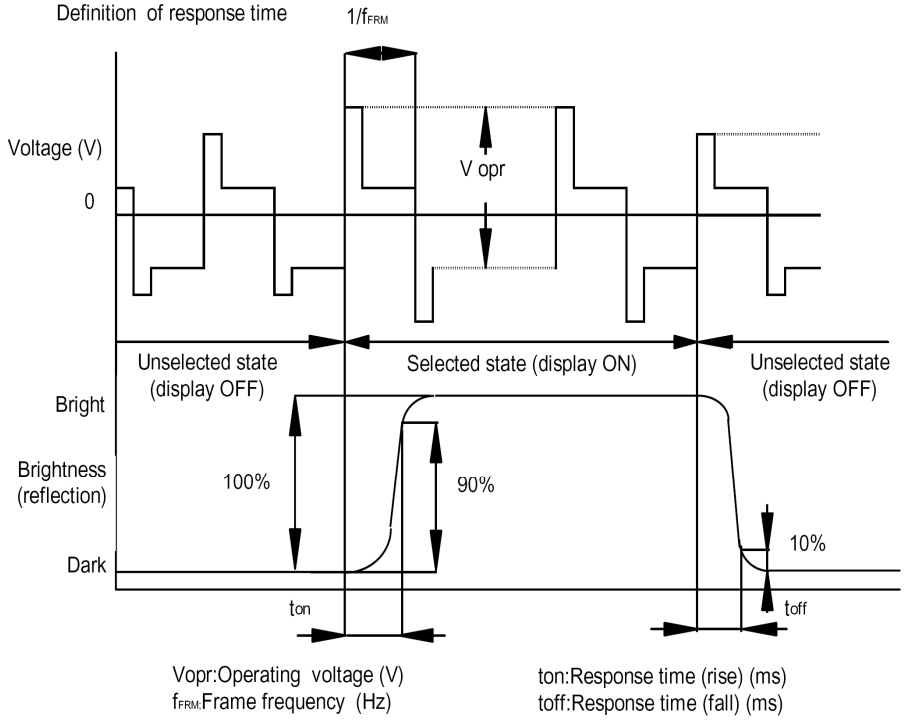


Definition of viewing angle

Definition of viewing angle θ1 and θ2

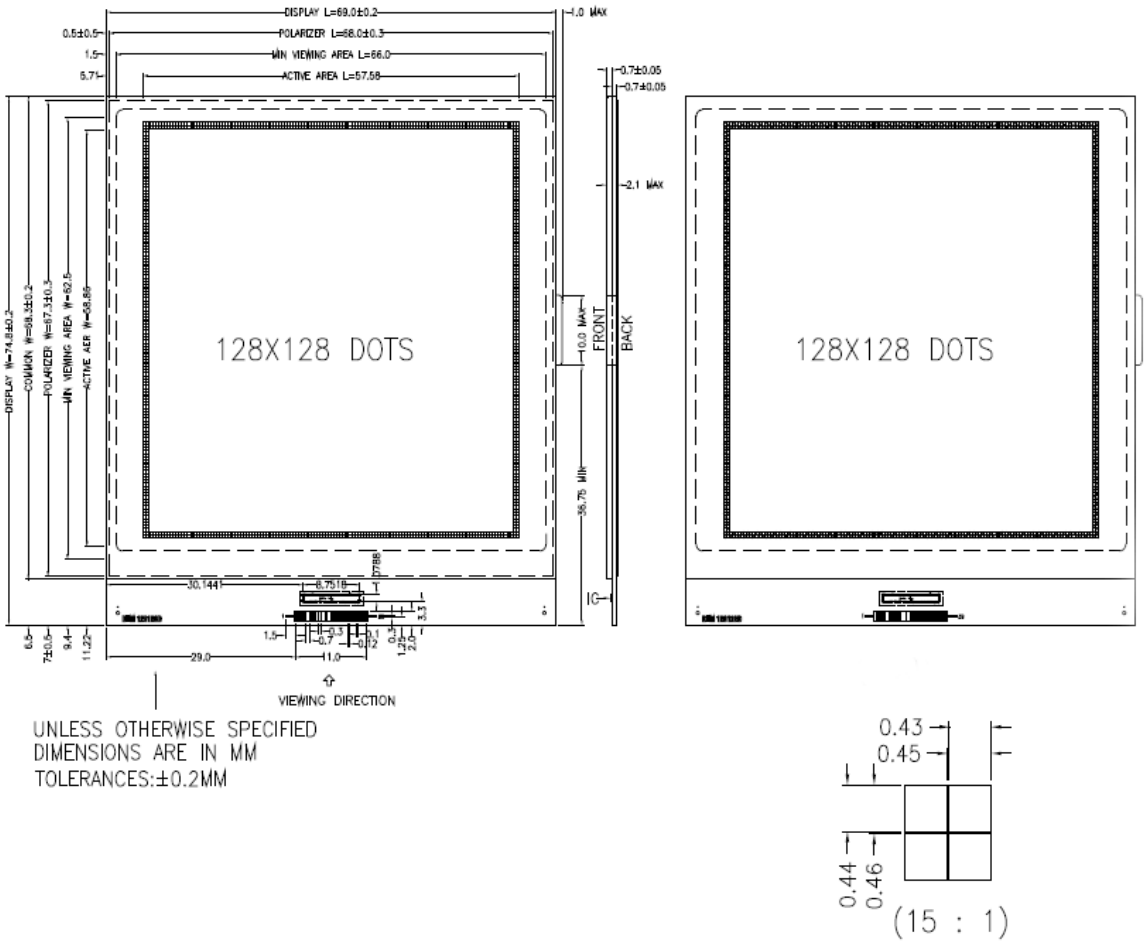


Definition of response time

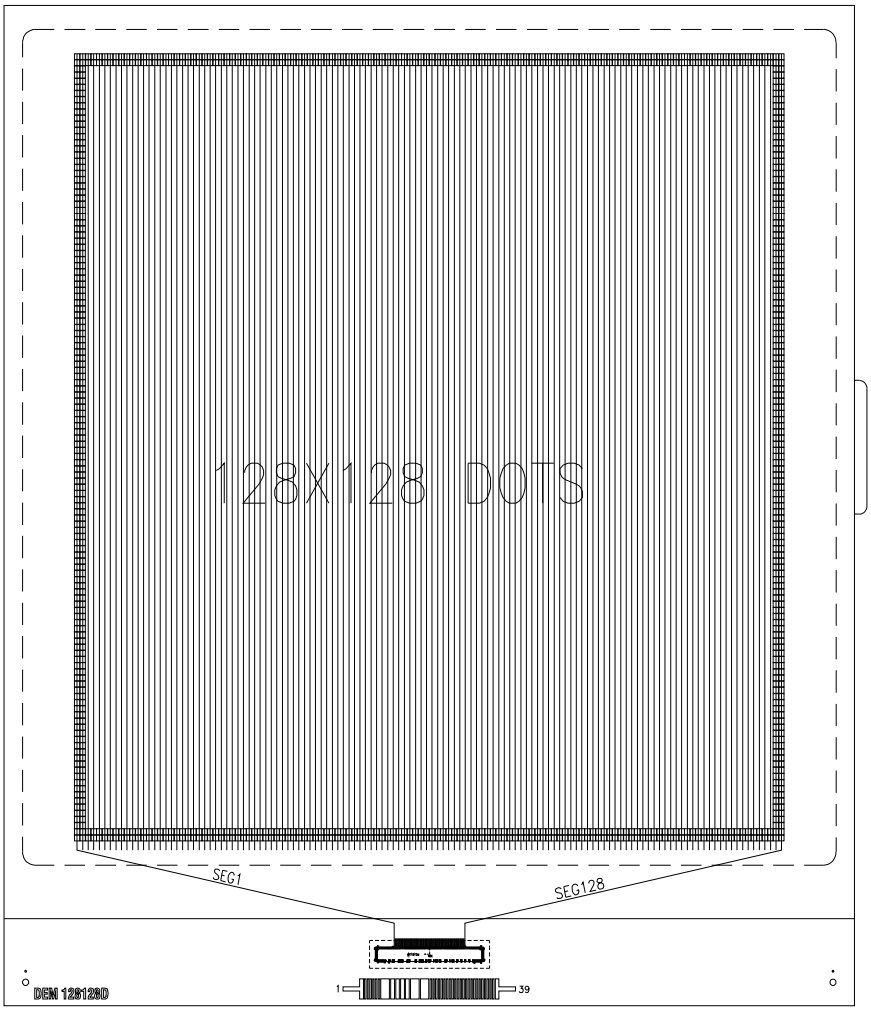


11. LCD DRAWING

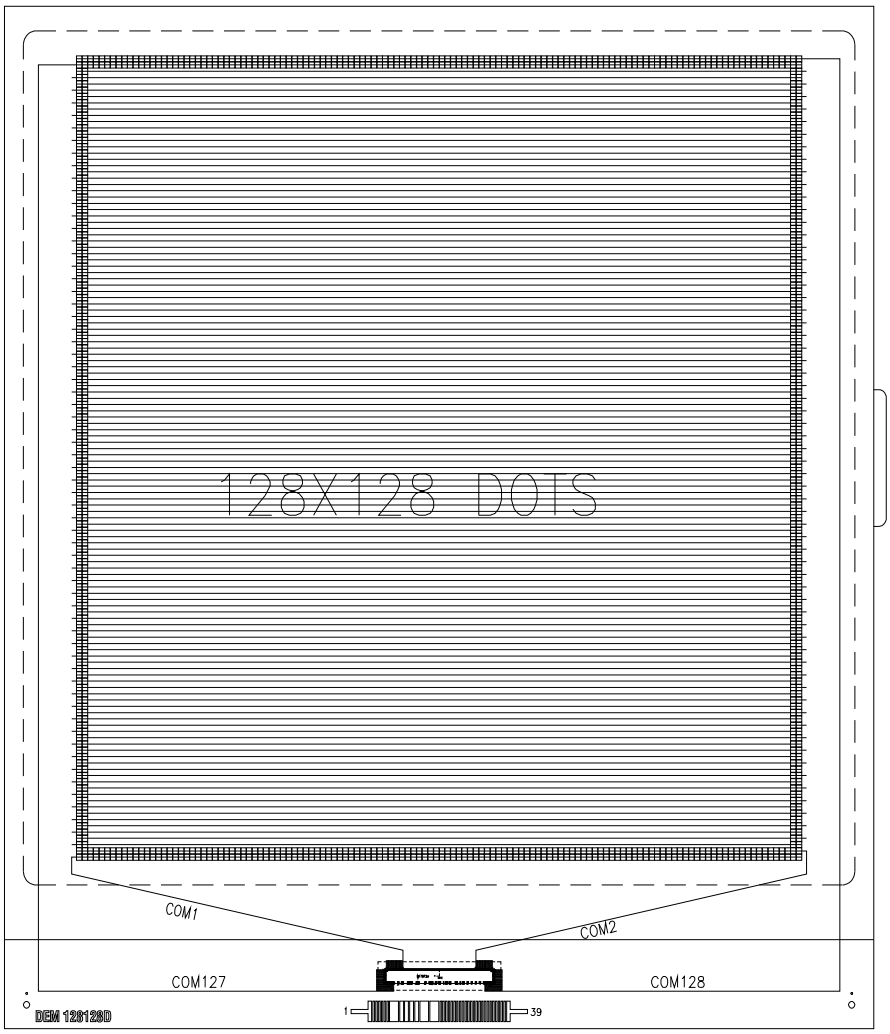
11.1. LCD ARTWORK



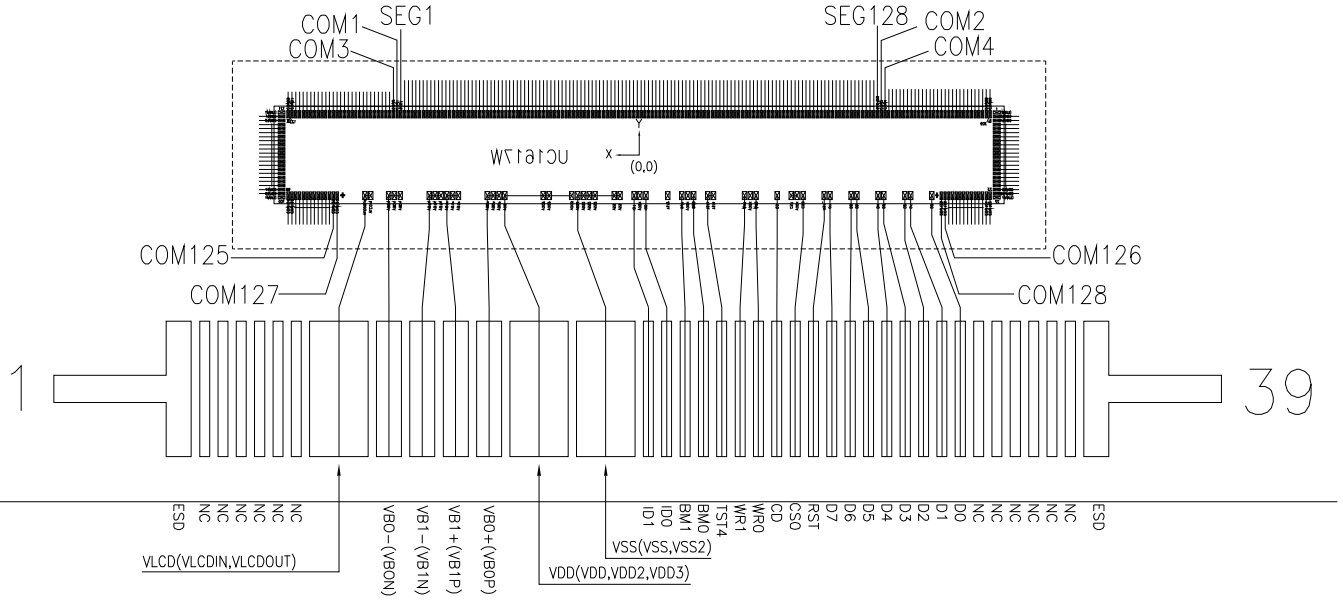
11.2. SEGMENT LAYOUT



11.3. COMMON LAYOUT



11.5. IC LAYOUT

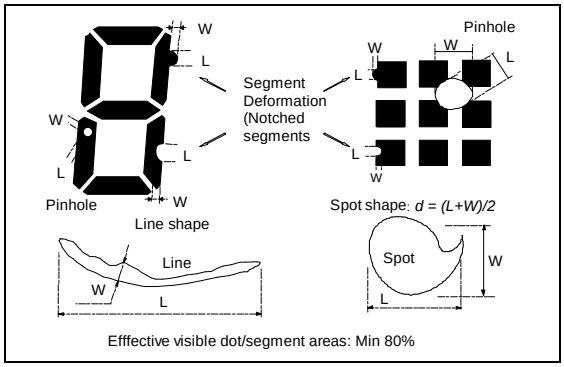


12. QUALITY DESCRIPTION

DEFECT SPECIFICATION:

Specific type-related items are covered in this sheet.

a: Table for Cosmetic defects
(Note: nc = not counted).
Sizes and number of defects
(Max. Qty)

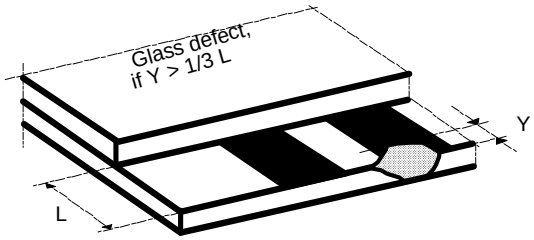


Defect Type	Max. defect size [µm] d or L W	Max. Quantity.
Black or White Spots	d ≤ 150	nc
	150< d ≤ 300	5
Black or White Lines	-- W ≤ 10	nc
	L ≤ 5000 W ≤ 30	3
	L ≤ 2000 W ≤ 50	2
Pinhole	d ≤ 150 150< d ≤ 300	nc 1/segment
(Total defects)		(5)
Segment Deformation	W ≤ 100	nc
Bubble (e.g. under pola)	d ≤ 150	nc
	200< d ≤ 400	3
	400< d ≤ 600	1

Examples/ Shapes

b: Glass defects

b1:Glass defects at contact ledge



b2:Glass chipping in other areas shall not be in conflict with the product's function.

13. MODULE ACCEPT QUALITY LEVEL (AQL)

Inspection Standard: MIL-STD-105E Table Normal Inspection Single Sampling Level Ⅱ.

14. RELIABILITY TEST

Operating life time: 50,000 hours (at room temperature without direct irradiation of sunlight)
Reliability characteristics shall meet following requirements.

Tests Item	Condition
High Temperature Storage	+80°C x 96HR
Low Temperature Storage	-30°C x 96HR
High Temperature Operation	+70°C x 96HR
Low Temperature Operation	-20°C x 96HR
High Temperature, High humidity	+60°C x 90%RH x 96HR
Thermal Shock	-20°C x 30min à 25°C x 10s à +70°C x 30 min x 5 cycles
Vibration Test	Frequency x Swing x Time 40Hz x 4mm x 4hrs
Drop Test	Height x no. of drop 1.0m x 6 drops

15. LCD MODULES HANDLING PRECAUTIONS

- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.
- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.
- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

  -Be sure to ground the body when handling the LCD module.

  -Tools required for assembly, such as soldering irons, must be properly grounded.

  -To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

  -The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.
- Storage precautions

  When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below -20°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

16. OTHERS

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.
- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.
- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules:

  - Exposed area of the printed circuit board
  - Terminal electrode sections