

**DISPLAY Elektronik GmbH**

**DATA SHEET**

**LCD MODULE**

**DEM 128064I ADX-PW-N**

*Product Specification*

*Version: 5*

**13.07.2018**

# GENERAL SPECIFICATION

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MODULE NO. :

**DEM 128064I ADX-PW-N**

**CUSTOMER P/N:**

Version NO.	Change Description	Date
0	Original Version	15.06.2017
1	Change the LCD to Transmissive negative and change the OP./ST. Temperature	17.06.2017
2	Correct the module drawing on page 3 and correct BL drawing on page 7	14.09.2017
3	Correct the LCD operation voltage to 11.0V from 9 V in page 2/page 8	20.09.2017
4	Change the backlight temperature on page 7	09.04.2018
5	Cancel sentence in the drawing page 7	13.07.2018

PREPARED BY: HZ

DATE: 13.07.2018


APPROVED BY: MHO

DATE: 13.07.2018

**CONTENTS**

**1. FUNCTIONS & FEATURES ..... 2**

**2. MECHANICAL SPECIFICATIONS ..... 2**

**3. EXTERNAL DIMENSIONS (  UNIT: MM)..... 3**

**4. BLOCK DIAGRAM ..... 4**

**5. PIN ASSIGNMENT ..... 5**

**6. ABSOLUTE MAXIMUM RATINGS..... 6**

**7. BACKLIGHT ELECTRONICS/OPTICAL SPECIFICATIONS ..... 7**

**8. DC CHARACTERISTICS ..... 8**

**9. AC ELECTRICAL CHARACTERISTICS ..... 8**

**10. COMMAND TABLE ..... 11**

**11. ACCEPT QUALITY LEVEL (AQL)..... 12**

**12. RELIABILITY TEST ..... 12**

**13. QUALITY DESCRIPTION..... 13**

**14. LCD MODULES HANDLING PRECAUTIONS ..... 14**

**15. OTHERS ..... 14**

**1. FUNCTIONS & FEATURES**

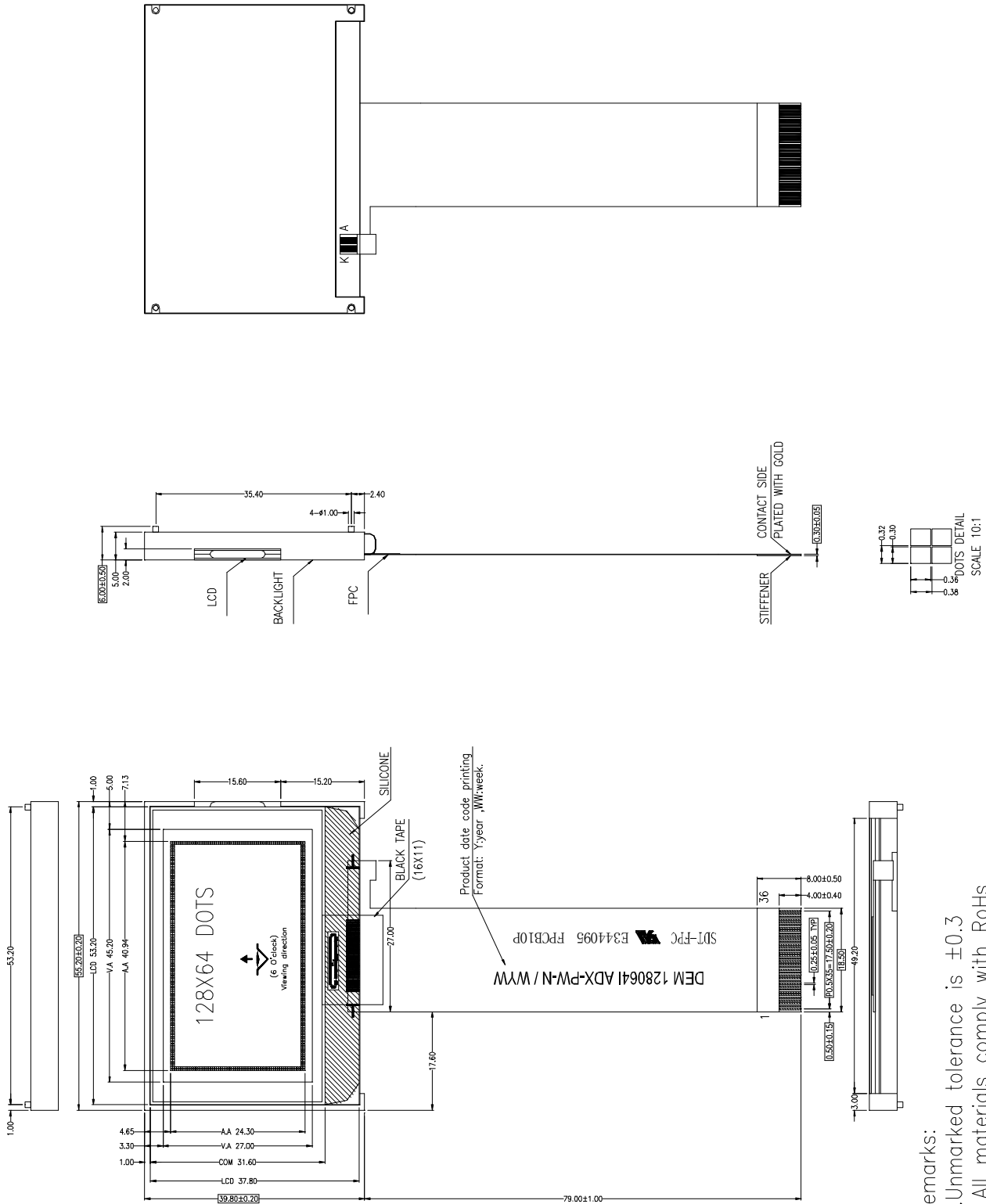
<b>Module</b>	<b>LCD Type</b>	<b>Remark</b>
DEM 128064I ADX-PW-N	ASTN Transmissive Negative Mode	

- Viewing Direction : 6 O'clock
- Driving Scheme : 1/65Duty Cycle, 1/9 Bias
- Power Supply Voltage : 3.3 V
- LCD Operation Voltage(V0-VSS) : 11.0 V
- Driver IC : ST7565P
- Display Contents : 128x 64 Dots
- Interface : Parallel & Serial
- RoHS : Compliant

**2. MECHANICAL SPECIFICATIONS**

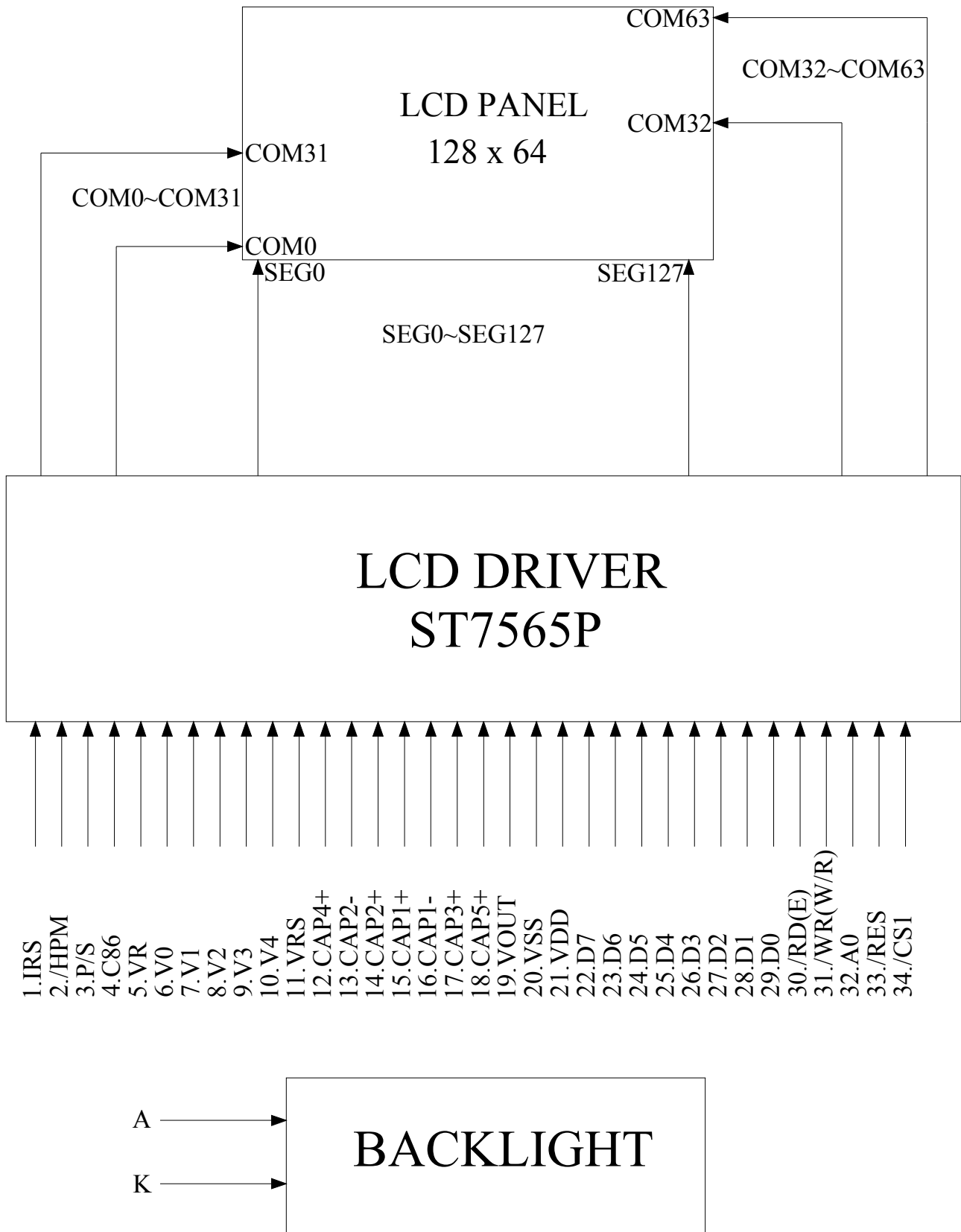
- Module Size(Without FPC) : 55.20 x 39.80 x 5.00 mm
- View Area : 45.20 x 27.00 mm
- Active Area : 40.94 x 24.30 mm
- Dot Size : 0.30 x 0.36 mm
- Dot Pitch : 0.32 x 0.38 mm
- Dot Gap : 0.02 mm

3. EXTERNAL DIMENSIONS (  unit: mm)



- Remarks:
1. Unmarked tolerance is ±0.3
  2. All materials comply with RoHS
  3.   ....critical dimension.

4. BLOCK DIAGRAM



## 5. PIN ASSIGNMENT

Pin No.	Name	Description																														
1	IRS	This terminal selects the resistors for the V0 voltage level adjustment. IRS = "H": Use the internal resistors IRS = "L": Do not use the internal resistors. The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal																														
2	/HPM	This is the power control terminal for the power supply circuit for liquid crystal drive. /HPM = "H": Normal mode /HPM = "L": High power mode																														
3	P/S	This pin configures the interface to be parallel mode or serial mode. P/S = "H": Parallel data input/output. P/S = "L": Serial data input. When P/S = "L", D0 to D5 must be fixed to "H". /RD (E) and /WR (R/W) are fixed to either "H" or "L".																														
4	C86	This is the MPU interface selection pin. C86 = "H": 6800 Series MPU interface. C86 = "L": 8080 Series MPU interface.																														
5	VR	Output voltage regulator terminal. Provides the voltage between VSS and V0 through a resistive voltage divider. IRS = "L": the V0 voltage regulator internal resistors are not used. IRS = "H": the V0 voltage regulator internal resistors are used.																														
6	V0	This is multi-level power supply for liquid crystal drive. Voltage levels are determined based on VDD, and must maintain the relative magnitudes show below.																														
7	V1	$V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS$																														
8	V2	Master operation when the power supply turns on, the internal power supply circuits produce V1 to V4 voltage shown below. The voltage setting are selected using the LCD bias set command.																														
9	V3	<table border="1"> <thead> <tr> <th></th> <th>1/65 DUTY</th> <th>1/49 DUTY</th> <th>1/33 DUTY</th> <th>1/55 DUTY</th> <th>1/53 DUTY</th> </tr> </thead> <tbody> <tr> <td>V1</td> <td><math>8/9 * V0, 6/7 * V0</math></td> <td><math>7/8 * V0, 5/6 * V0</math></td> <td><math>5/6 * V0, 4/5 * V0</math></td> <td><math>7/8 * V0, 5/6 * V0</math></td> <td><math>7/8 * V0, 5/6 * V0</math></td> </tr> <tr> <td>V2</td> <td><math>7/9 * V0, 5/7 * V0</math></td> <td><math>6/8 * V0, 4/6 * V0</math></td> <td><math>4/6 * V0, 3/5 * V0</math></td> <td><math>6/8 * V0, 4/6 * V0</math></td> <td><math>6/8 * V0, 4/6 * V0</math></td> </tr> <tr> <td>V3</td> <td><math>2/9 * V0, 2/7 * V0</math></td> <td><math>2/8 * V0, 2/6 * V0</math></td> <td><math>2/6 * V0, 2/5 * V0</math></td> <td><math>2/8 * V0, 2/6 * V0</math></td> <td><math>2/8 * V0, 2/6 * V0</math></td> </tr> <tr> <td>V4</td> <td><math>1/9 * V0, 1/7 * V0</math></td> <td><math>1/8 * V0, 1/6 * V0</math></td> <td><math>1/6 * V0, 1/5 * V0</math></td> <td><math>1/8 * V0, 1/6 * V0</math></td> <td><math>1/8 * V0, 1/6 * V0</math></td> </tr> </tbody> </table>		1/65 DUTY	1/49 DUTY	1/33 DUTY	1/55 DUTY	1/53 DUTY	V1	$8/9 * V0, 6/7 * V0$	$7/8 * V0, 5/6 * V0$	$5/6 * V0, 4/5 * V0$	$7/8 * V0, 5/6 * V0$	$7/8 * V0, 5/6 * V0$	V2	$7/9 * V0, 5/7 * V0$	$6/8 * V0, 4/6 * V0$	$4/6 * V0, 3/5 * V0$	$6/8 * V0, 4/6 * V0$	$6/8 * V0, 4/6 * V0$	V3	$2/9 * V0, 2/7 * V0$	$2/8 * V0, 2/6 * V0$	$2/6 * V0, 2/5 * V0$	$2/8 * V0, 2/6 * V0$	$2/8 * V0, 2/6 * V0$	V4	$1/9 * V0, 1/7 * V0$	$1/8 * V0, 1/6 * V0$	$1/6 * V0, 1/5 * V0$	$1/8 * V0, 1/6 * V0$	$1/8 * V0, 1/6 * V0$
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V2	$7/9 * V0, 5/7 * V0$	$6/8 * V0, 4/6 * V0$	$4/6 * V0, 3/5 * V0$	$6/8 * V0, 4/6 * V0$	$6/8 * V0, 4/6 * V0$																											
V3	$2/9 * V0, 2/7 * V0$	$2/8 * V0, 2/6 * V0$	$2/6 * V0, 2/5 * V0$	$2/8 * V0, 2/6 * V0$	$2/8 * V0, 2/6 * V0$																											
V4	$1/9 * V0, 1/7 * V0$	$1/8 * V0, 1/6 * V0$	$1/6 * V0, 1/5 * V0$	$1/8 * V0, 1/6 * V0$	$1/8 * V0, 1/6 * V0$																											
10	V4																															
11	VRS	This is the internal-output VREG power supply for the LCD power supply voltage regulator.																														
12	CAP4+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2-terminal.																														
13	CAP2-	DC/DC voltage converter. Connects a capacitor between this terminal and CAP2+ terminal.																														
14	CAP2+	DC/DC voltage converter. Connects a capacitor between this terminal and CAP2-terminal.																														
15	CAP1+	DC/DC voltage converter. Connects a capacitor between this terminal and CAP1-terminal.																														
16	CAP1-	DC/DC voltage converter. Connects a capacitor between this terminal and CAP1+ terminal.																														
17	CAP3+	DC/DC voltage converter. Connects a capacitor between this terminal and CAP1-terminal.																														
18	CAP5+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1-terminal.																														
19	VOUT	DC/DC voltage converter. Connects a capacitor between this terminal and VSS or VDD																														

		terminal.
20	VSS	Ground
21	VDD	Power supply
22	D7	<p>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.</p> <p>When the serial interface (SPI-4) is selected (P/S = "L"):  D7: serial data input (SI); D6: the serial clock input (SCL).  D0 to D5 should be connected to VDD or floating.  When the chip select is not active, D0 to D7 are set to high impedance.</p>
23	D6	
24	D5	
25	D4	
26	D3	
27	D2	
28	D1	
29	D0	
30	/RD (E)	<ul style="list-style-type: none"> <li>When connected to 8080 series MPU, this pin is treated as the "/RD" signal of the 8080 MPU and is LOW-active.</li> </ul> <p>The data bus is in an output status when this signal is "L".</p> <ul style="list-style-type: none"> <li>When connected to 6800 series MPU, this pin is treated as the "E" signal of the 6800 MPU and is HIGH-active.</li> </ul> <p>This is the enable clock input terminal of the 6800 Series MPU.</p>
31	/WR (R/W)	<ul style="list-style-type: none"> <li>When connected to 8080 series MPU, this pin is treated as the "/WR" signal of the 8080 MPU and is LOW-active.</li> </ul> <p>The signals on the data bus are latched at the rising edge of the /WR signal.</p> <ul style="list-style-type: none"> <li>When connected to 6800 series MPU, this pin is treated as the "R/W" signal of the 6800 MPU and decides the access type :  When R/W = "H": Read.  When R/W = "L": Write.</li> </ul>
32	A0	<p>This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command.</p> <p>A0="HIGH": indicates that D0 to D7 are display data.  A0="LOW": indicates that D0 to D7 are control data.</p>
33	/RES	<p>When /RES is set to LOW, the settings are initialed.</p> <p>The reset operation is performed by the /RES signal level.</p>
34	/CS1	<p>This is the chip select signal for first chip.</p> <p>when /CS1=LOW, the chip select becomes active and the data/commands I/O is enabled</p>
35	K	LED-
36	A	LED+

## 6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	VDD	0.3 ~ 3.6	V
Power Supply Voltage (VDD standard)	VDD2	0.3 ~ 3.6	V
Power Supply Voltage (VDD standard)	V0, VOUT	0.3 ~ 14.5	V
Power Supply Voltage (VDD standard)	V1, V2, V3, V4	V0 to 0.3	V
Operating Temperature	Topr	-30 to +80	°C
Storage Temperature	Tstr	-40 to +90	°C

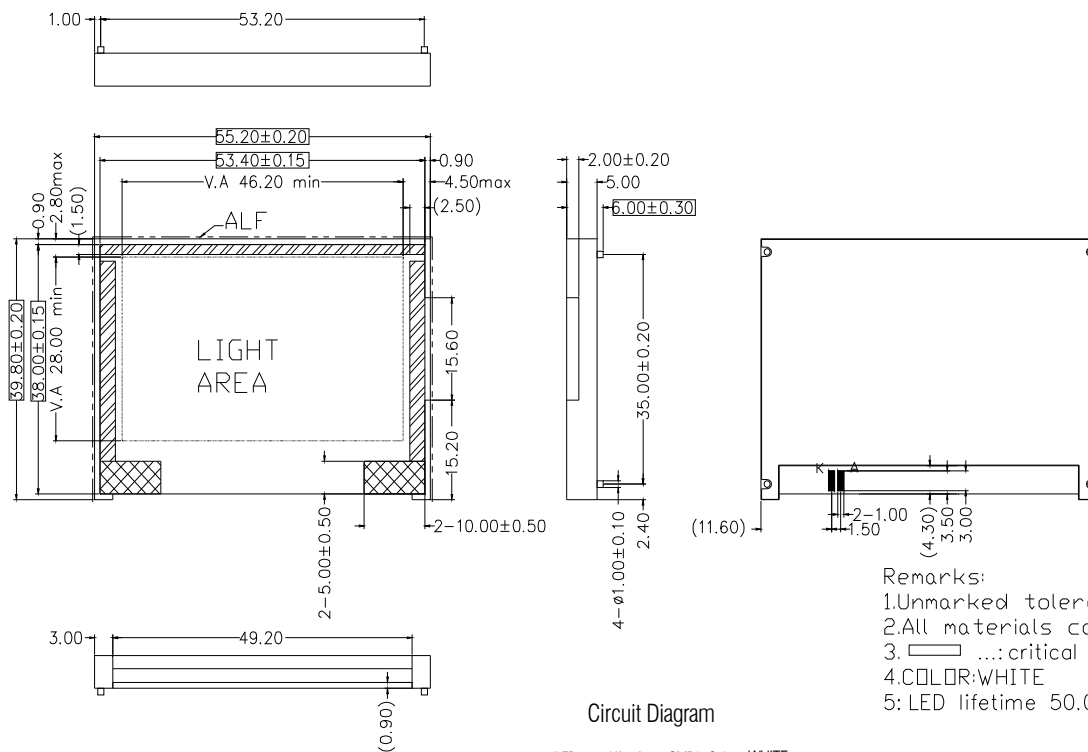


7. BACKLIGHT ELECTRONICS/OPTICAL SPECIFICATIONS

Item	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Forward Current	I <sub>f</sub>	--	45	60	mA	V <sub>f</sub> = 3.3 V
Colour Coordinate (Tolerance:±0.01)	X	0.26		0.33		
	Y	0.26		0.33		
Luminance	L <sub>v</sub>	400	600	900	cd/m <sup>2</sup>	TEST INSTRUMENT
Uniformity	Avg	70	---	---	%	
Reverse Current	I <sub>r</sub>			15	uA	V <sub>r</sub> = 5 V

● Operating Temperature: -30~+80°C    ● Storage Temperature: -40~+90°C

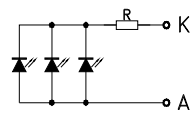
▨ TESA 4980    ▩ TESA 4968



- Remarks:
- 1.Unmarked tolerance is ±0.3
  - 2.All materials comply with RoHs
  - 3.▭ ...:critical dimension.
  - 4.COLOR:WHITE
  - 5: LED lifetime 50.000 hours

Circuit Diagram

(LED 1X3=3 SMD) Color: WHITE



8. DC CHARACTERISTICS

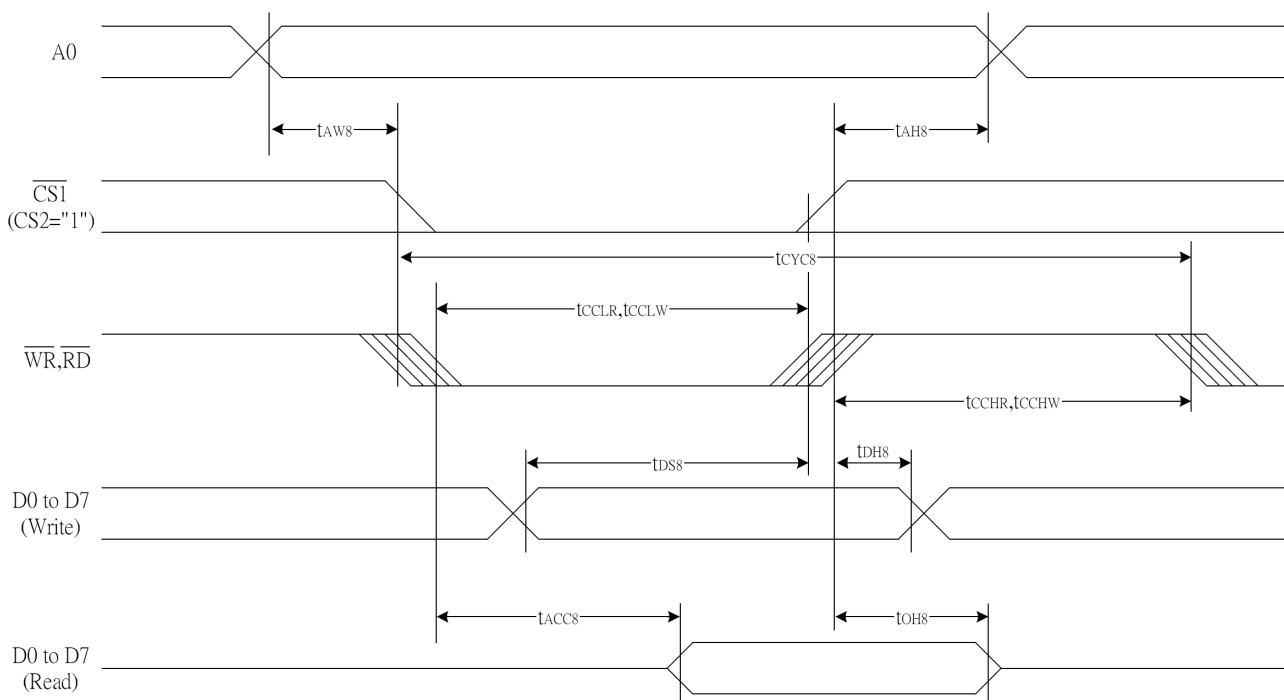
Item	Symbol	Standard Value			Test Condition	Unit
		Min.	Typ.	Max.		
Power supply Voltage	V <sub>DD</sub>	3.0	3.3	3.6	V <sub>0</sub> -V <sub>SS</sub>	V
Operating Voltage	V <sub>LCD</sub>	10.7	11	11.3		
Current Consumption	I <sub>DD</sub>	---	170	255		uA

9. AC ELECTRICAL CHARACTERISTICS

9.1 System bus READ/WRITE characteristics for the 8080 series MPU

(V<sub>DD</sub>=3.3V, V<sub>SS</sub>=0V)

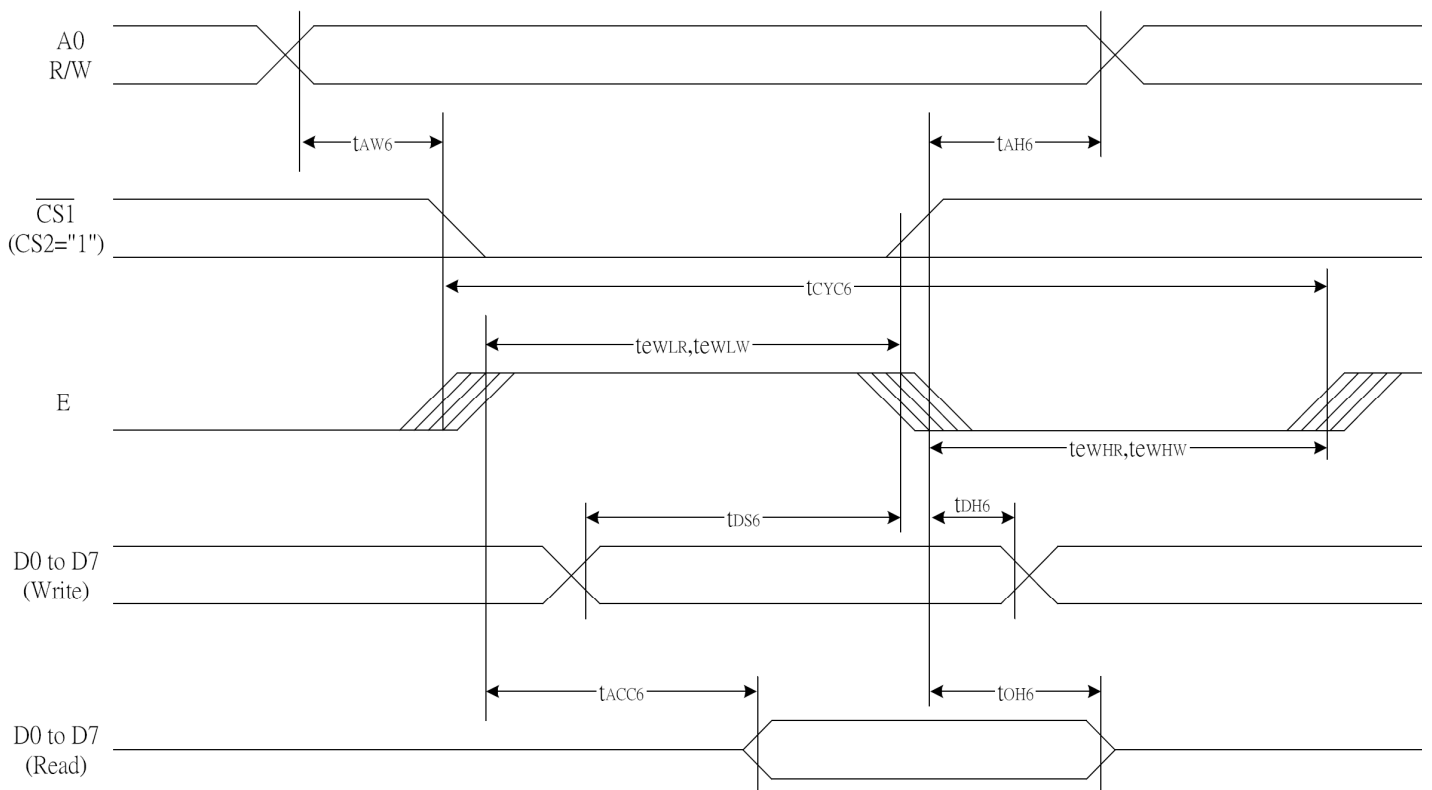
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t <sub>AH8</sub>		0	—	ns
Address setup time		t <sub>AW8</sub>		0	—	
System cycle time		t <sub>CYC8</sub>		240	—	
Enable L pulse width (WRITE)	WR	t <sub>CCLW</sub>		80	—	
Enable H pulse width (WRITE)		t <sub>CCHW</sub>		80	—	
Enable L pulse width (READ)	RD	t <sub>CCLR</sub>		140	—	
Enable H pulse width (READ)		t <sub>CCHR</sub>		80	—	
WRITE Data setup time	D0 to D7	t <sub>DS8</sub>		40	—	
WRITE Address hold time		t <sub>DH8</sub>		0	—	
READ access time		t <sub>ACC8</sub>	CL = 100 pF	—	70	
READ Output disable time		t <sub>OH8</sub>	CL = 100 pF	5	50	



9.2 System bus READ/WRITE characteristics for the 6800 series MPU

(VDD=3.3V, VSS=0V)

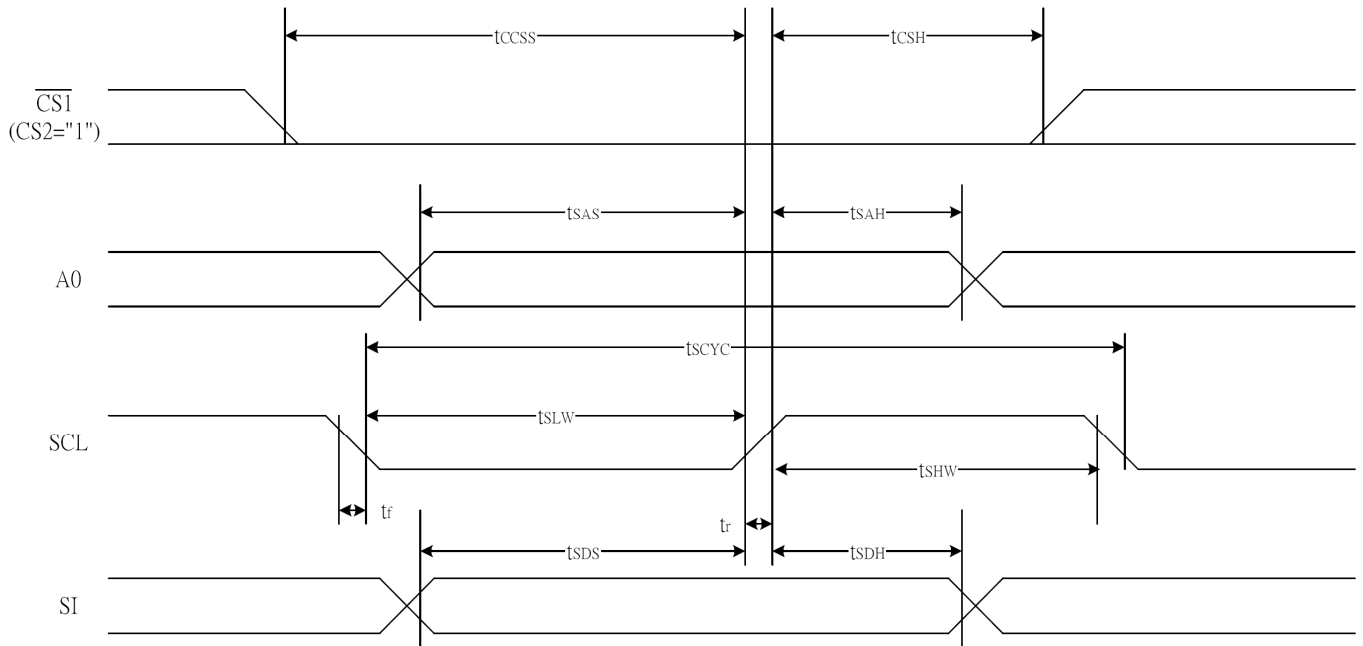
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	$t_{AH6}$		0	—	ns
Address setup time		$t_{AW6}$		0	—	
System cycle time		$t_{CYC6}$		240	—	
Enable L pulse width (WRITE)	WR	$t_{EWLW}$		80	—	
Enable H pulse width (WRITE)		$t_{EWHW}$		80	—	
Enable L pulse width (READ)	RD	$t_{EWLR}$		80	—	
Enable H pulse width (READ)		$t_{EWHR}$		140	—	
WRITE Data setup time	D0 to D7	$t_{DS6}$		40	—	
WRITE Address hold time		$t_{DH6}$		0	—	
READ access time		$t_{ACC6}$	CL = 100 pF	—	70	
READ Output disable time		$t_{OH6}$	CL = 100 pF	5	50	



9.3 The Serial Interface

(VDD=3.3V, VSS=0V)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	$t_{SCYC}$		50	—	ns
SCL “H” pulse width		$t_{SHW}$		25	—	
SCL “L” pulse width		$t_{SLW}$		25	—	
Address setup time	A0	$t_{SAS}$		20	—	
Address hold time		$t_{SAH}$		10	—	
Data setup time	SI	$t_{SDS}$		20	—	
Data hold time		$t_{SDH}$		10	—	
CS-SCL time	CS	$t_{CSS}$		20	—	
CS-SCL time		$t_{CSH}$		40	—	



## 10. COMMAND TABLE

Command	Table of ST7565P Commands										Function		
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1		D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address	
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address	
(4) Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.	
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address					
(5) Status read	0	0	1	Status				0	0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM	
(7) Display data read	1	0	1	Read data								Reads from the display RAM	
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0	1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0	1	Sets the LCD display normal/reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0	1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0	1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565P)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0	*	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode	
(17) V <sub>0</sub> voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode	
(18) Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	0	1	Set the V <sub>0</sub> output voltage electronic volume register
Electronic volume register set				0	0	Electronic volume value							
(19) Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0	1	0: OFF, 1: ON
Static indicator register set				0	0	0	0	0	0	0	0	0	Mode
(20) Booster ratio set	0	1	0	1	1	1	1	1	0	0	0	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power saver													Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	*	Command for IC test. Do not use this command

**11. ACCEPT QUALITY LEVEL (AQL)**

11.1 AQL Standard Value: Critical Defect =0.1, Major Defect=0.65; Minor Defect =2.5.

11.2 Inspection Plan: MIL-STD-105E, Normal Inspection Level II, Single Sampling Plan.

**12. RELIABILITY TEST**

Operating life time: 50,000 hours (at room temperature without direct irradiation of sunlight)

Reliability characteristics shall meet following requirements.

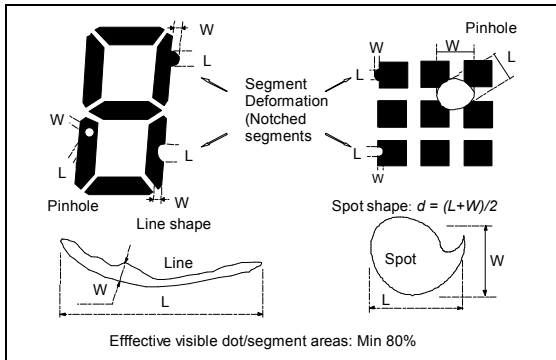
<b>Test Item</b>	<b>Test Condition</b>
High temperature storage	+90°C x 96hrs
Low temperature storage	-40°C x 96hrs
High temperature operation	+80°C x 96hrs
Low temperature operation	-30°C x 96hrs
High temperature, High humidity	+60° x 90%RH x 96hrs
Thermal shock	-30°C x 30min → +25°C x 10s → +80°C x 30min 5 Cycles
Vibration test	Frequency x Swing x Time 40Hz x 4mm x 4hrs
Drop test	Drop height x No. of drops 1.0m x 6drops

13. QUALITY DESCRIPTION

**DEFECT SPECIFICATION:**

a: Table for Cosmetic defects

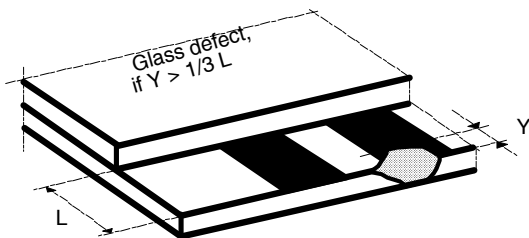
(Note: nc = not counted).  
 Sizes and number of defects  
 (Max. Qty)



Examples/ Shapes

b: Glass defects

b1: Glass defects at contact ledge



b2: Glass chipping in other areas shall not be in conflict with the product's function.

Defect Type	Max. defect size [μm] d or L W	Max. Quantity.
Black or White Spots	$d \leq 100$	nc
	$150 < d \leq 300$	3
Black or White Lines	$W \leq 10$	nc
	$L \leq 3000$ $W \leq 30$	2
	$L \leq 2000$ $W \leq 50$	2
Pinhole	$d \leq 100$	nc
	$150 < d \leq 300$	1/segment
(Total defects)		(5)
Segment Deformation	$W \leq 100$	nc
Bubble (e.g. under pola)	$d \leq 150$	nc
	$200 < d \leq 400$	2

**14. LCD MODULES HANDLING PRECAUTIONS**

- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.
- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.
- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

-Be sure to ground the body when handling the LCD module.

-Tools required for assembly, such as soldering irons, must be properly grounded.

-To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

-The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

- **Storage precautions**

When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

**15. OTHERS**

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.
- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.
- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules :
  - Exposed area of the printed circuit board
  - Terminal electrode sections